The Trigger System

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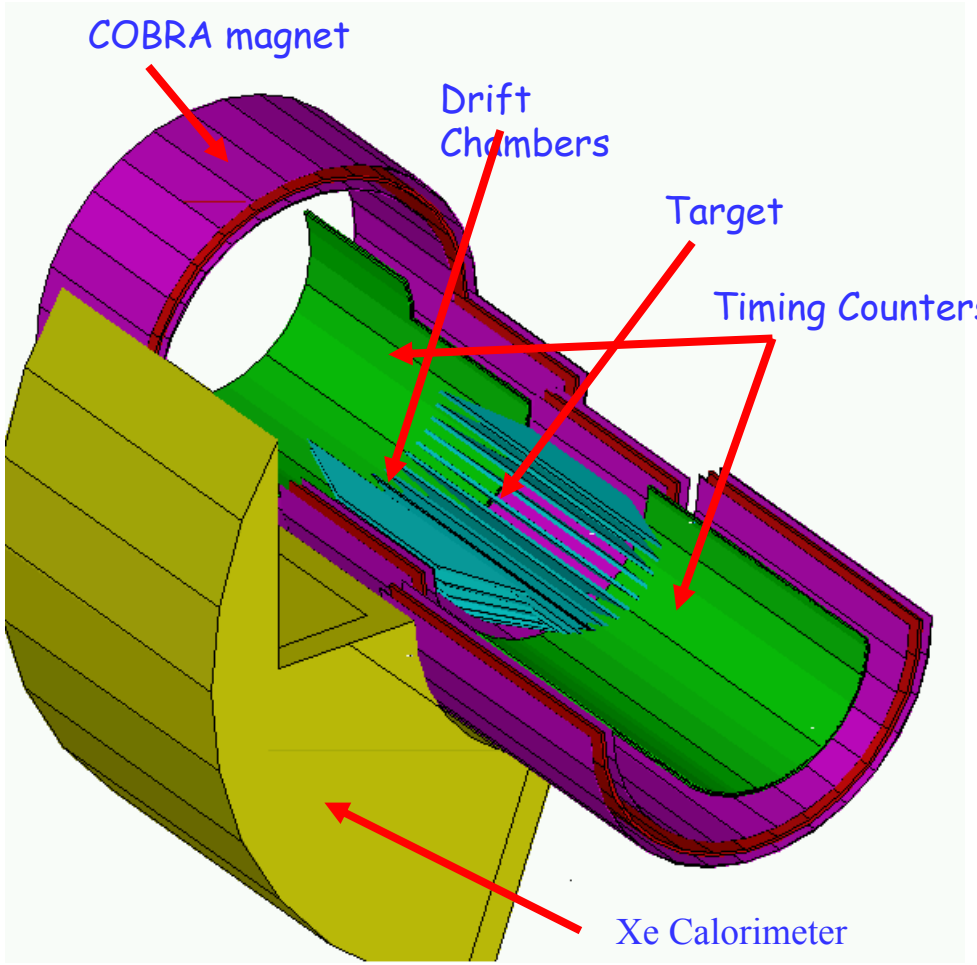
Background Rate Evaluation



- Simulation
  - Complete detector simulation with GEANT 3.21
  - Proposal geometry
- Contribution
  - correlated: irrelevant $\mu \to e \upsilon \upsilon \gamma$
  - accidental: main

$\mu \to e \upsilon \bar{\upsilon} \gamma$ and $\mu \to e \upsilon \bar{\upsilon}$

$e^+ e^- \to \gamma\gamma$

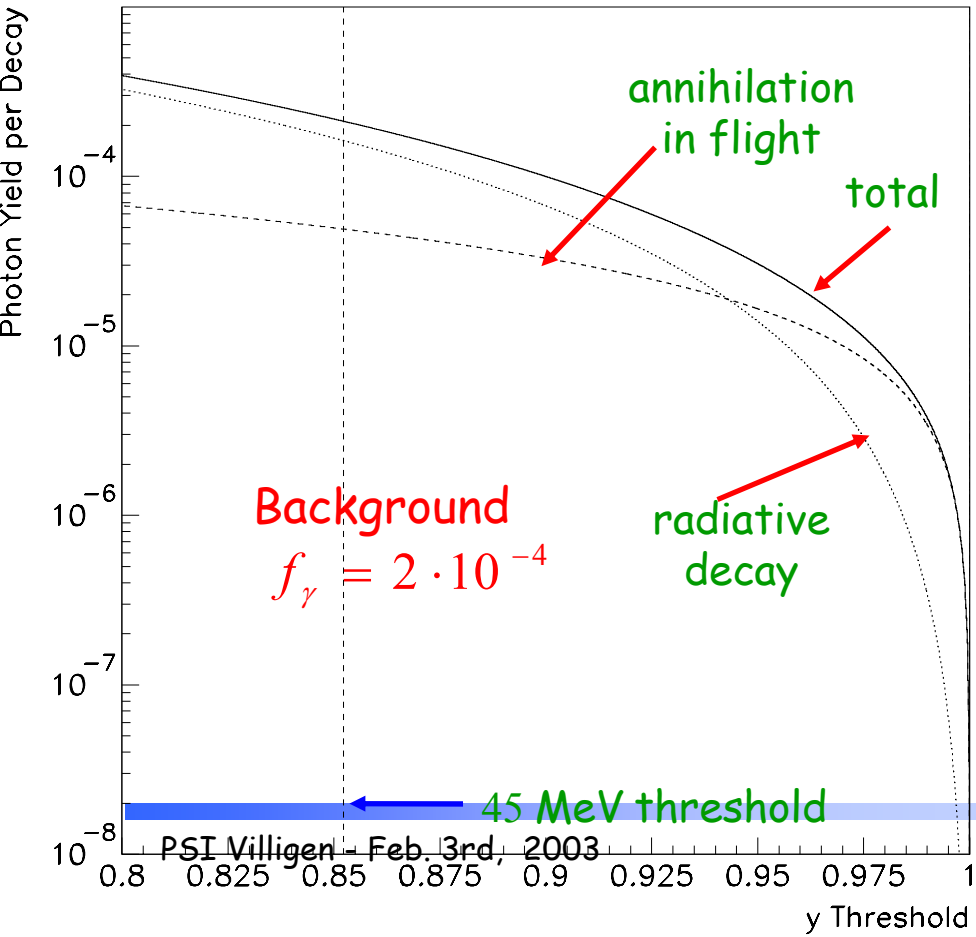
Trigger algorithms

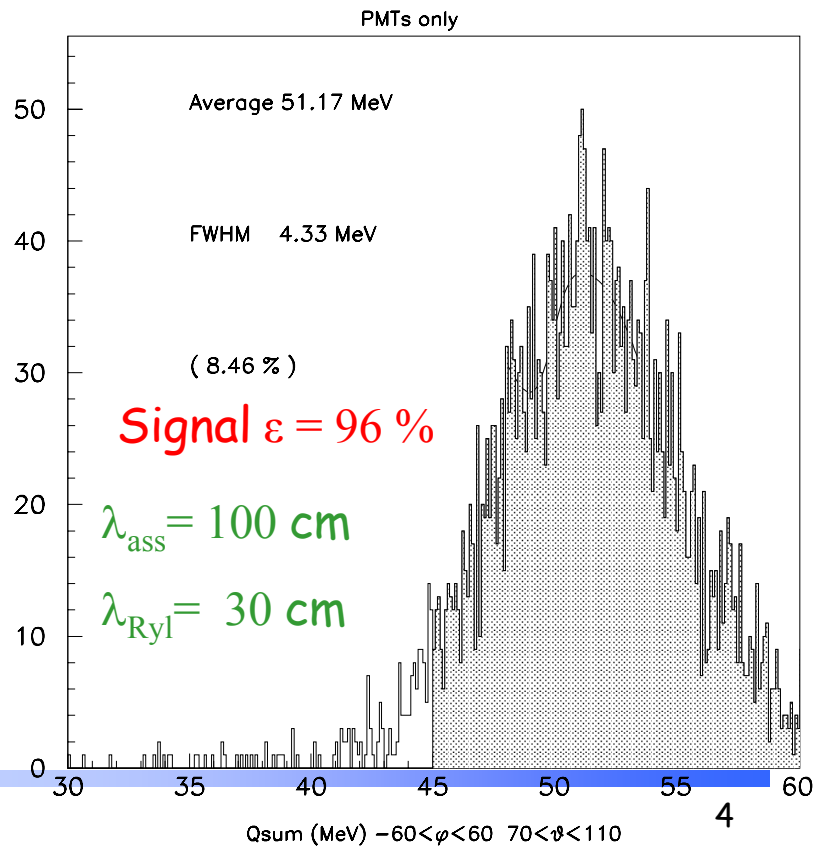
Physical variables	Detectors
a - photon energy b - photon direction c - photon time	**Liquid Xe calorimeter** - entrance face : needed for energy, direction and time - other faces : relevant only for the energy OK
d - positron direction e - positron time	**Timing Counters** - Counters along Z for the time - Position of the impact point on the counter for the direction OK
f - positron energy	**Tracking chambers** - Information delayed with respect to LXe and TC - Large number of channels - May be useful at a Second Level trigger NO

Photon Energy

baseline approach

$$QSUM = \sum_{i}^{N} w_i \, Q_i \qquad w_i = \text{PMT coverage density} \qquad Q_i = \text{i - th PMT charge}$$

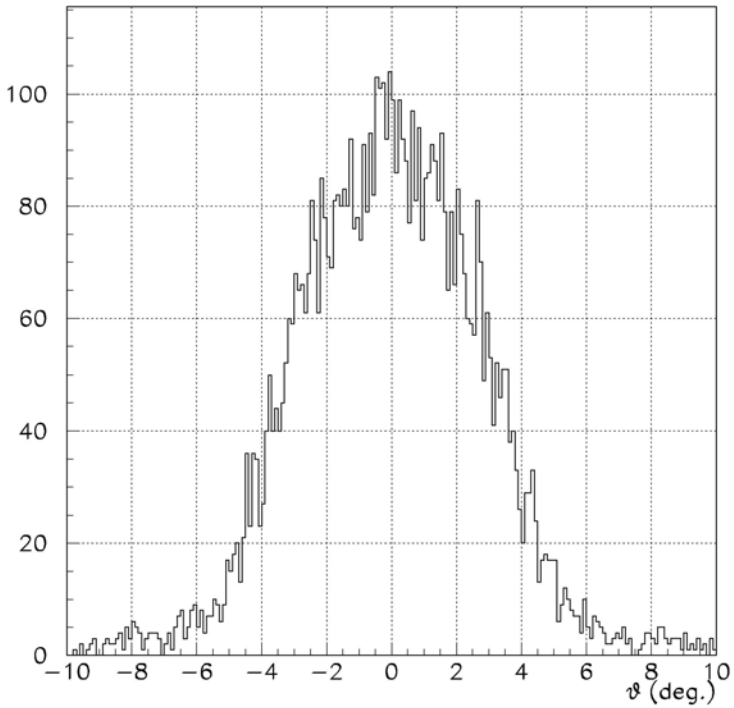


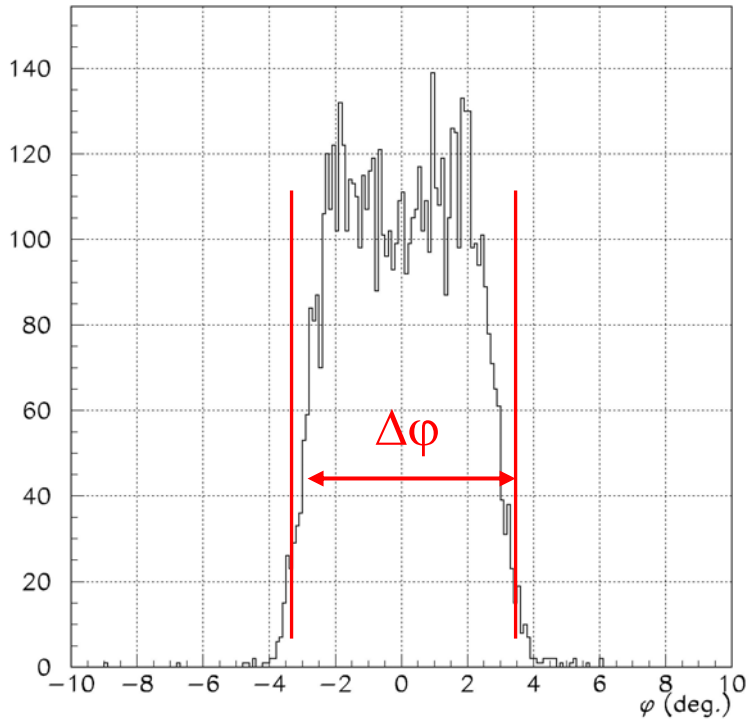


Photon Direction

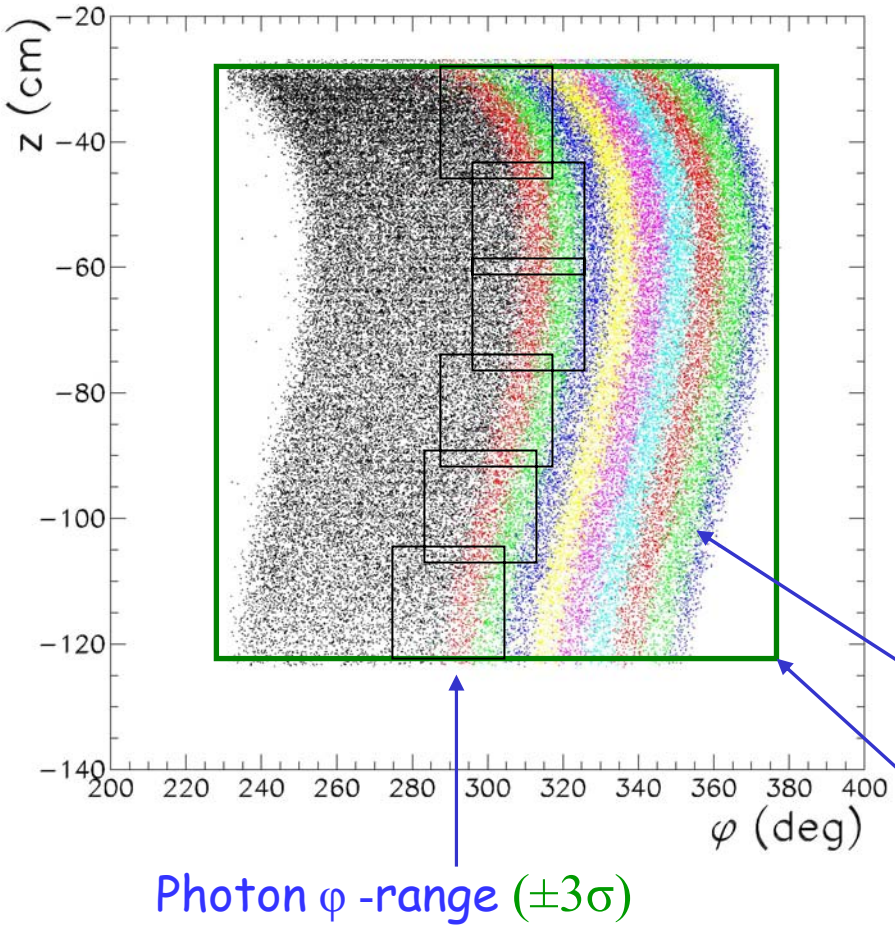
Maximum charge PMT on the entrance calorimeter face

highly efficient on the signal $\varepsilon\ (|\Delta\varphi| < 3.5°) \approx 99\%$





Positron photon direction matching



- 2 Timing Counters
  - Suppression factor for the θ coordinate $f_\theta = 2$
- φ - bands matching
  - Suppression factor for the φ coordinate $f_\varphi = 5$

γ - e^+ timing

Baseline approach of the time measurement

- assuming leading edge with at least 2 samplings (>20 ns)
- at least 2 consecutive voltage values above threshold
- look for changes of derivative sign
- perform a linear interpolation to compute the event time

$$10\left(V_{thr}-V_{i-3}\right)=\left(V_{i-1}-V_{i-2}\right)\left(t_{thr}-t_{i-3}\right)$$

$$2\,k\left(V_{i-1}-V_{i-2}\right)<\left(V_{thr}-V_{i-3}\right)<2\left(k+1\right)\left(V_{i-1}-V_{i-2}\right)$$

$$t_{thr}=\left(t_{i-3}+2\;k+1\right)$$

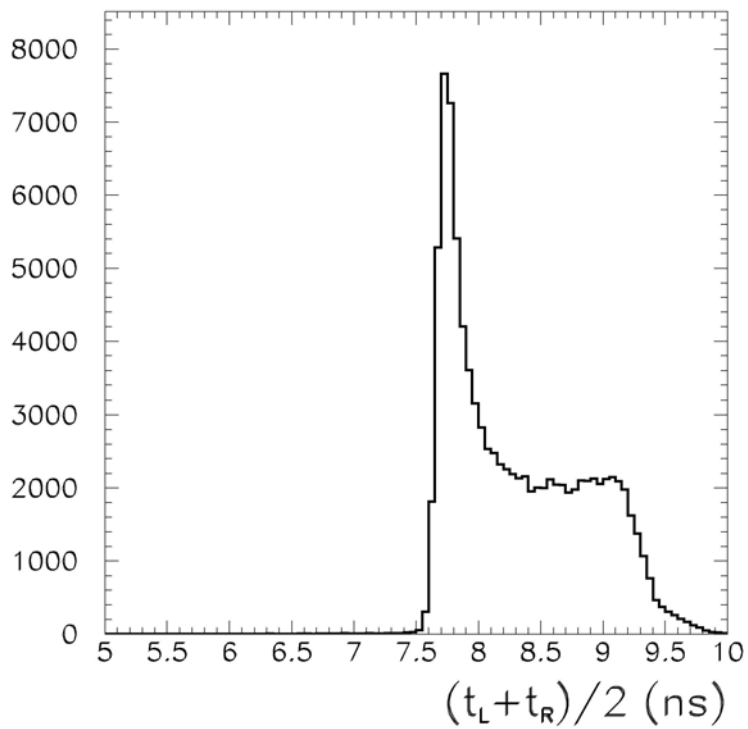
  - some ns accuracy
  - fixed delay (120 ns) between the time measurement and the pulse maximum amplitude

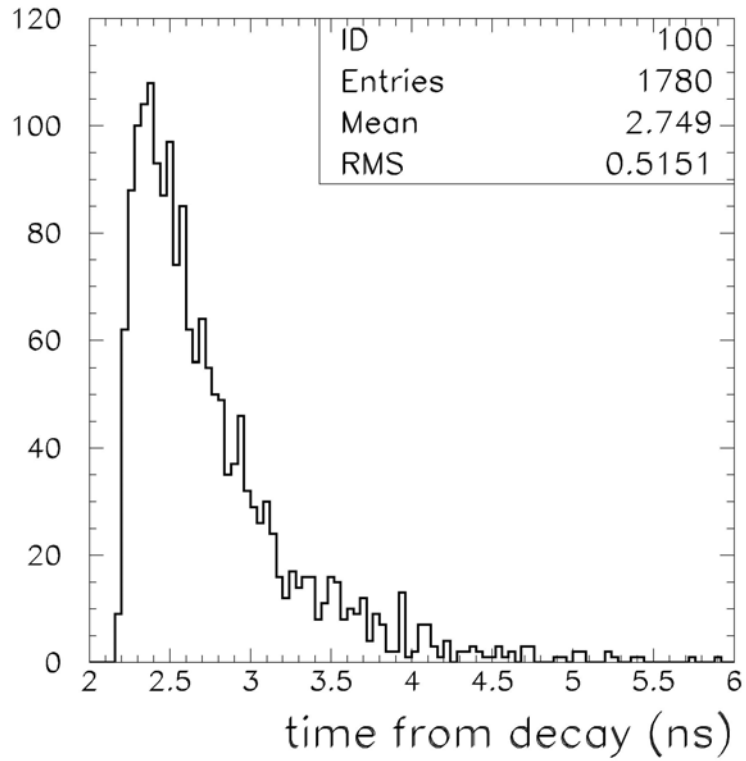
Possible simplification

- linear combination of consecutive sampling differences

Time coincidence

Safe choice: ΔT = 10 ns coincidence window





Trigger Rates Summary

Accidental background $\mu \to e \upsilon \bar{\upsilon} \gamma$ / $e^+e^- \to \gamma\gamma$ and $\mu \to e \upsilon \bar{\upsilon}$

rejection obtained by applying cuts on the following variables

- photon energy $E_\gamma > 45\ \mathrm{MeV} \Rightarrow \varepsilon \cong 97\% \quad f_\gamma \sim 2 \cdot 10^{-4}$
- photon direction $\sigma_\phi = 1.2^o \Rightarrow \varepsilon(\Delta\phi < 3.5^o) > 99\%$
- hit on the positron counter $\Rightarrow R_{e^+} = 5 \cdot 10^6\, s^{-1}$
- time correlation $\Delta T = 2 \times 10\ ns \Rightarrow \varepsilon \approx 100\%$
- positron-photon direction match $\Rightarrow f_\theta = 2\,;\, f_\varphi = 5$

$$R_\mu = 10^8\, s^{-1}$$

$$\frac{\Omega}{4\pi} = 0.1$$

$$R = R_\mu f_\gamma R_{e^+} \left(\frac{\Omega}{4\pi}\right)\left(\frac{\Delta T}{f_\vartheta f_\varphi}\right) \approx 20\ \mathrm{s}^{-1}$$

The rate depends on $R_\mu\, R_{e+} \propto R_\mu{}^2$

The trigger implementation

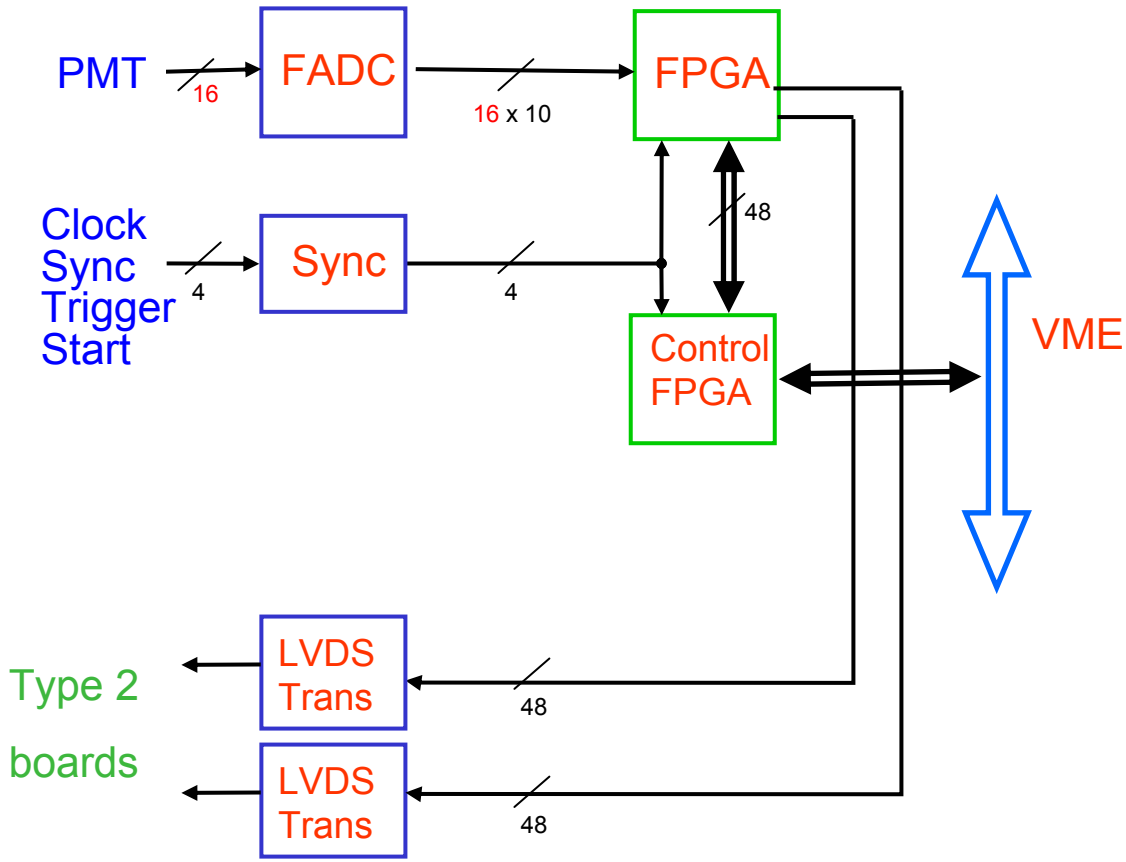
Digital approach

- Flash analog-to-digital converters (FADC)
- Field programmable gate array (FPGA)

Good reasons

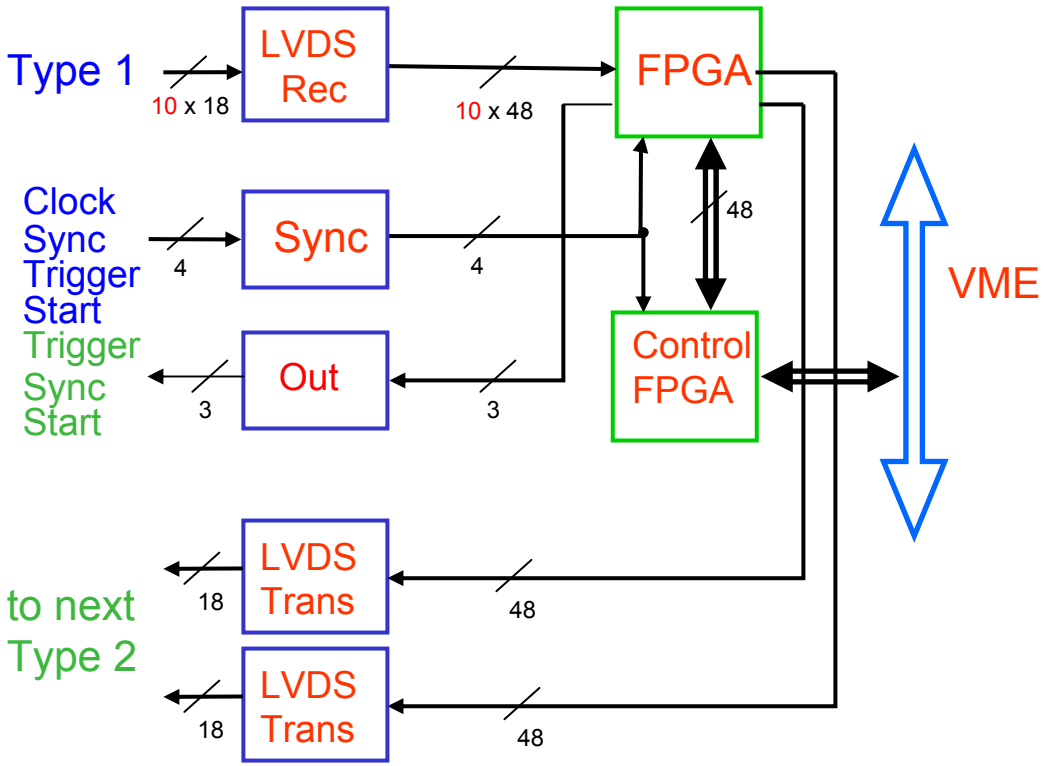
- Flexibility
- Complexity
- Common noise rejection
- Different reconstruction algorithms
- Easily and quickly reconfigurable

Hardware: board Type 1



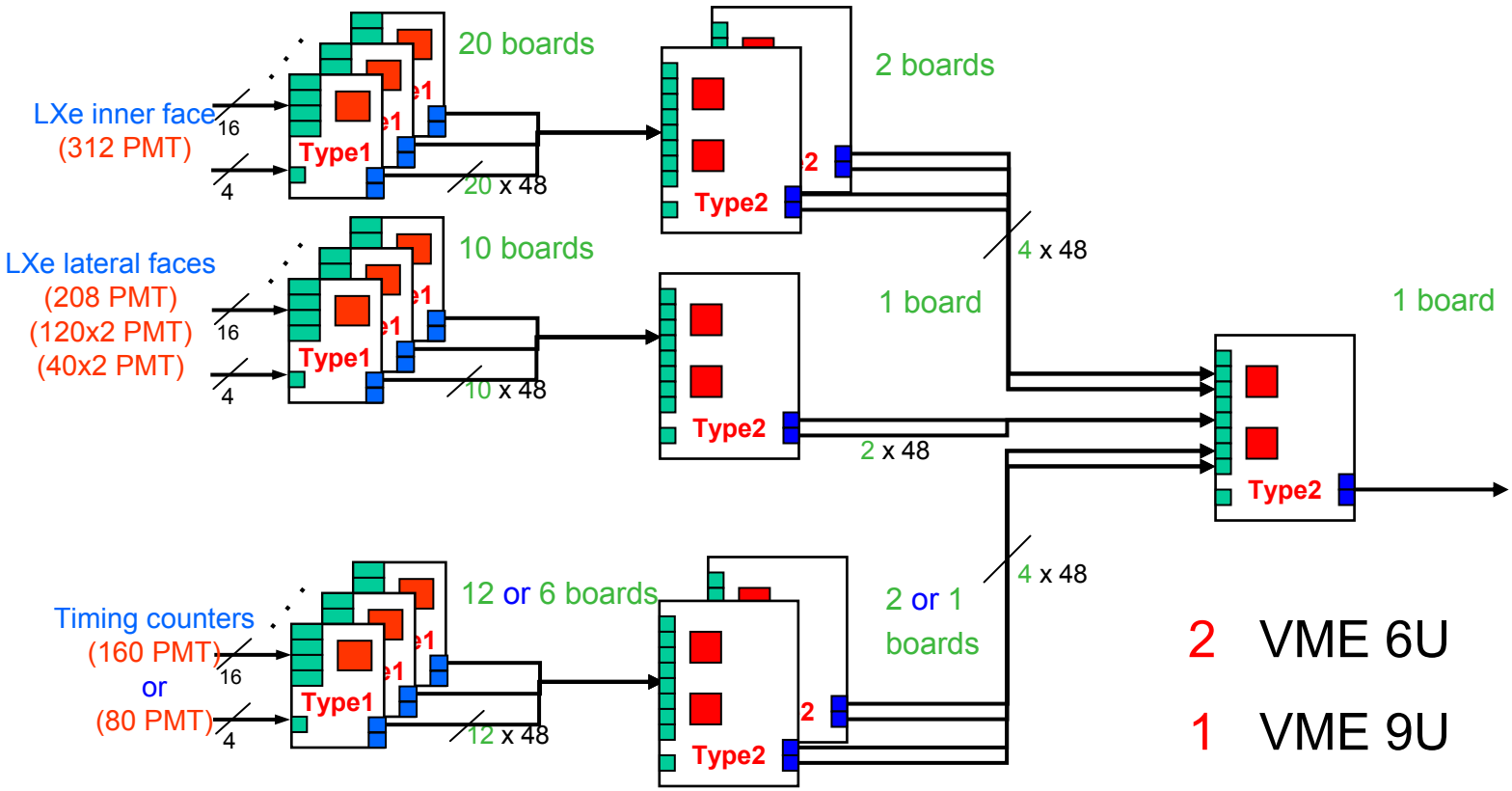
- VME 6U
- A-to-D Conversion
  - FADC with differential inputs bandwidth limited
- Trigger
  - LXe calorimeter
  - timing counters
- Acquisition
  - tracking chambers
- I/O
  - 16 PMT signals
  - 2 LVDS transmitters
  - 4 in control signals

Hardware: board Type 2



- VME 9U
- Matched with the Type 1 boards
- I/O
  - 10 LVDS receivers
  - 2 LVDS transmitters
  - 4 in control signals
  - 3 out signals

Hardware: system structure



Hardware: ancillary boards

- PMT fan-out for LXe Calorimeter and Timing Counters

  in: - single ended signal on 50 Ω coaxial cable

  out: - high quality signal to the digitizing electronic
  - output for control and debugging
  - 50 MHz bandwidth limited differential signal to the Type1 trigger board
  - 4 to 1 fan in capability for lateral faces

- Control signals fan-out for the trigger system

  Clock 10 MHz clock to all Type 1 and Type2 boards
  Sync high speed synchronization signal for timing measurement
  Start Run or control/debugging mode of the system

Trigger types

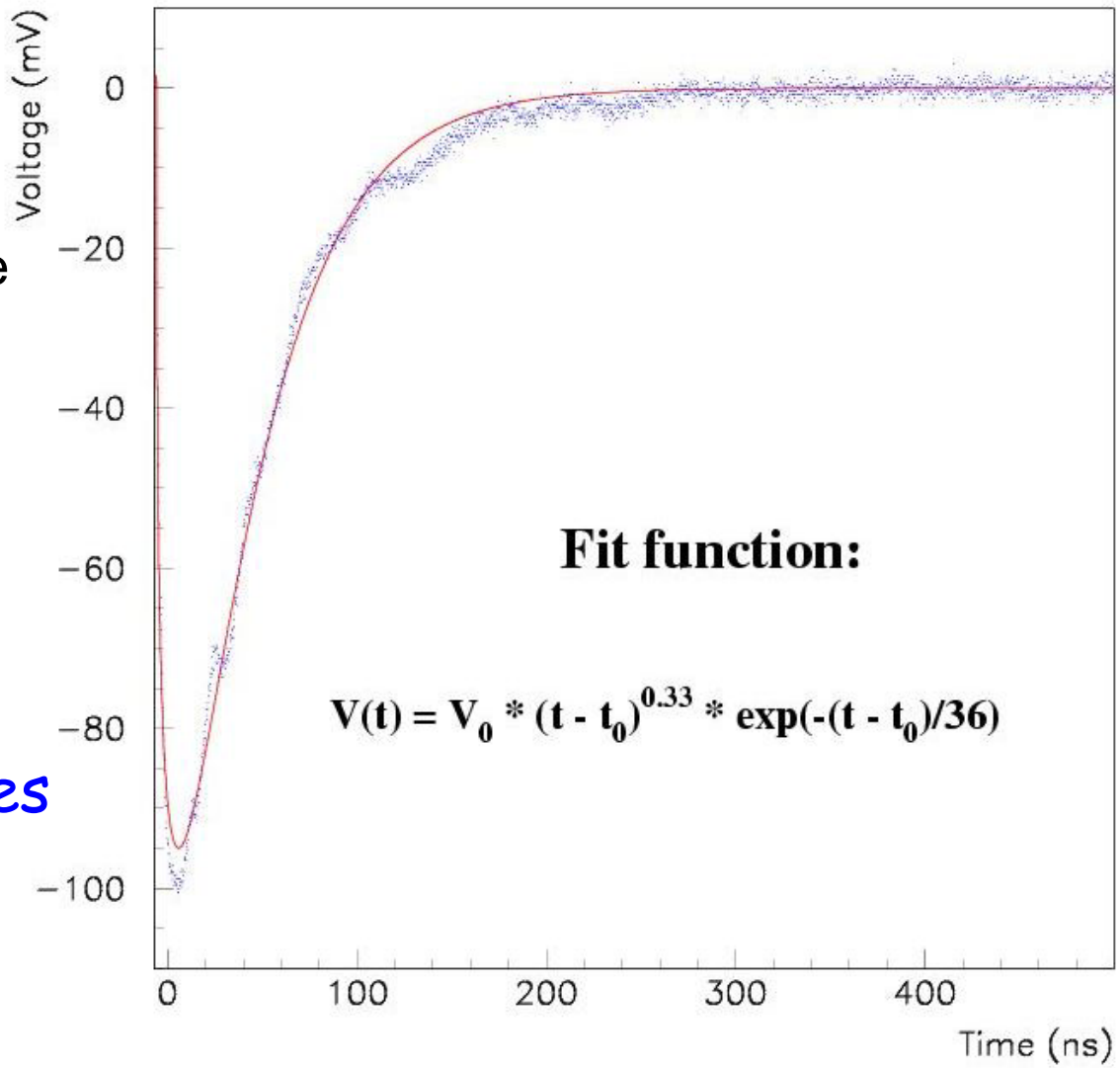
- Normal acquisition trigger
  - makes use of all variables of the photons and the positrons with baseline algorithms
- Debugging triggers
  - generated by relaxing 1 or 2 selection criteria at the time for a fraction of normal triggers
- Calibration triggers
  - connection of auxiliary external devices (calorimeters) through further Type1 boards
  - selection of $\mu \rightarrow e\nu\nu\gamma$ events for timing
- Different, more performing, triggers
  - hardware is dimensioned to support other algorithms (Principal Component Analysis)

Readout of the trigger system and detector status

- for each trigger the trigger configuration and status is read out
- for a fraction of the triggers the entire 100 MHz waveform buffers are read out
- for a fraction of the triggers the rates of each analog channel (LXe and TC) are readout

Trigger system simulation

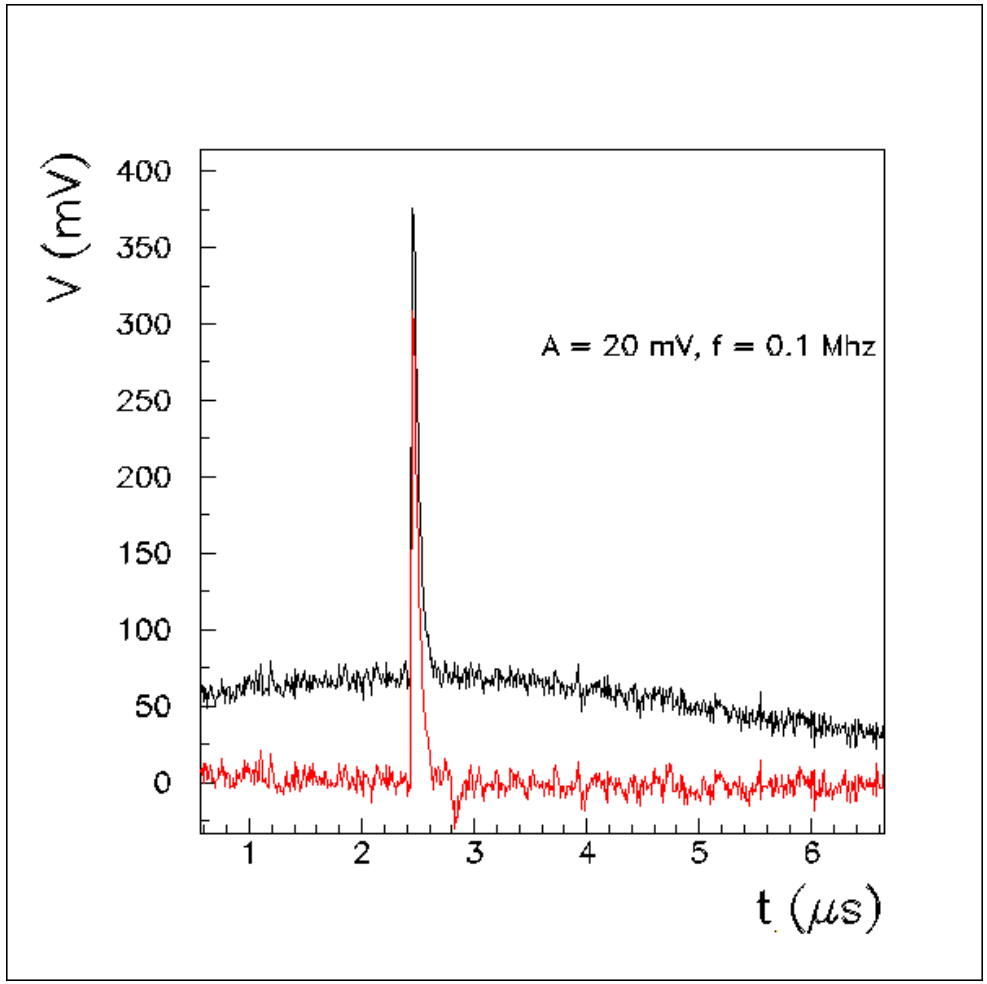
- PMT signals
  - Fit to a real PMT pulse of the large prototype
    +
  - Random noise
    +
  - Sinusoidal noise
- Simulation with abnormal noise figures



Pedestal and noise subtraction: 1

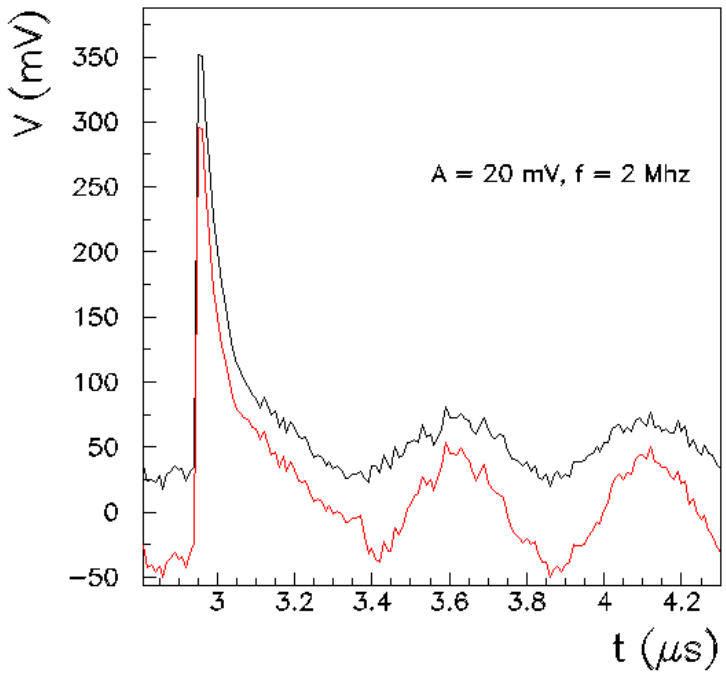
Excellent algorithm performance to suppress

- DC Pedestal
- Low frequency (<400KHz) noise

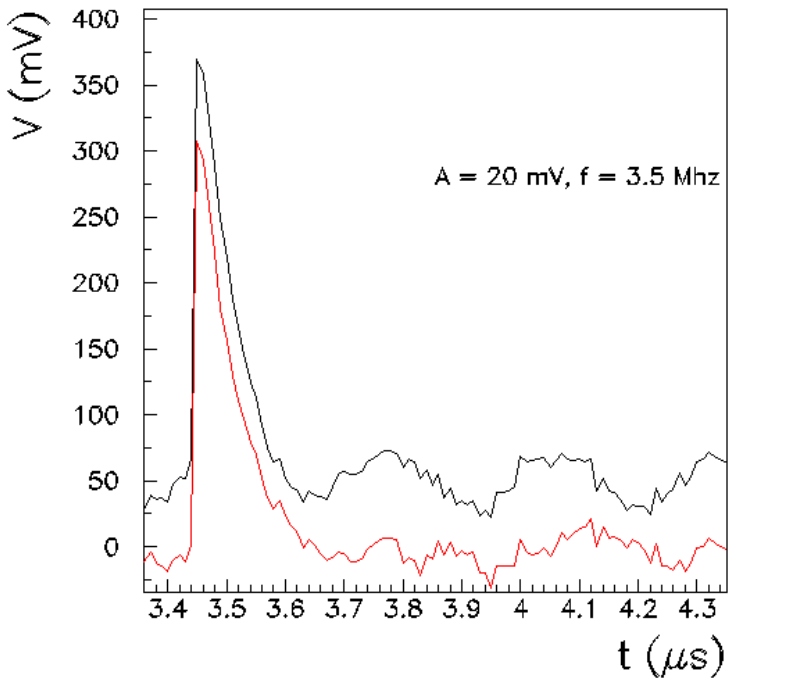


Pedestal and noise subtraction: 2

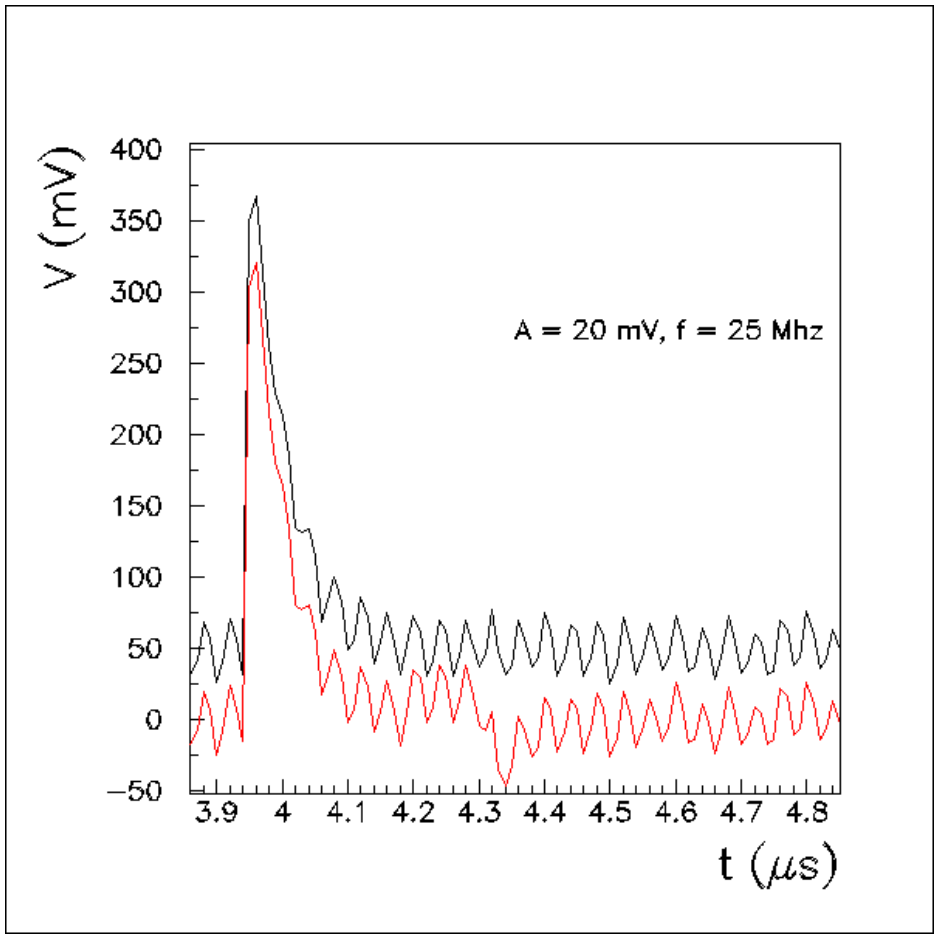
First critical frequency



First optimal frequency



Pedestal and noise subtraction: 3



High frequency noise (>15 MHz) is not amplified.

But

- FADC inputs must be bandwidth limited (at least <50MHz)
- The critical frequency can be tuned in the range 1-4 MHz, after having measured the real noise level

Other algorithms

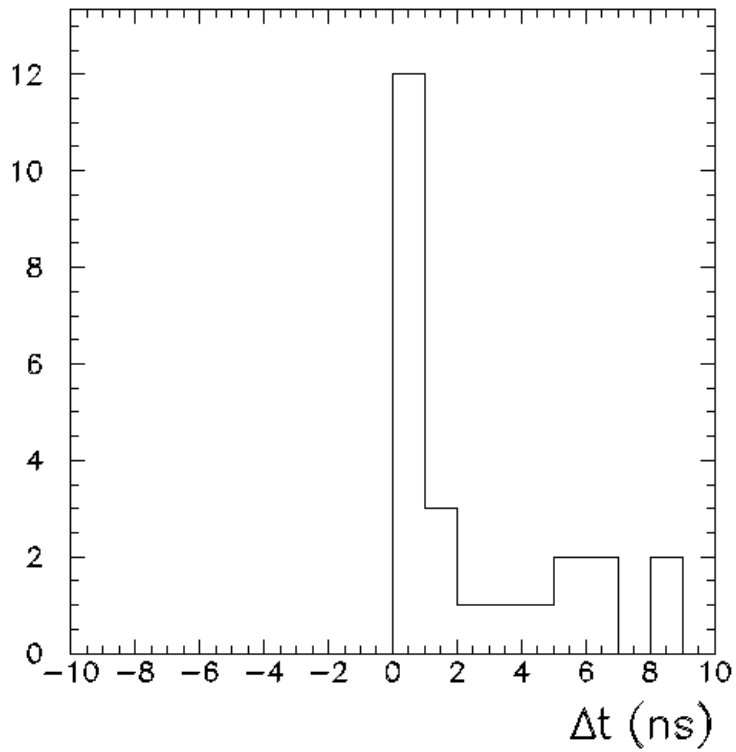
- The charge sum algorithm

and

- The maximum charge PMT search

do not have difficulties

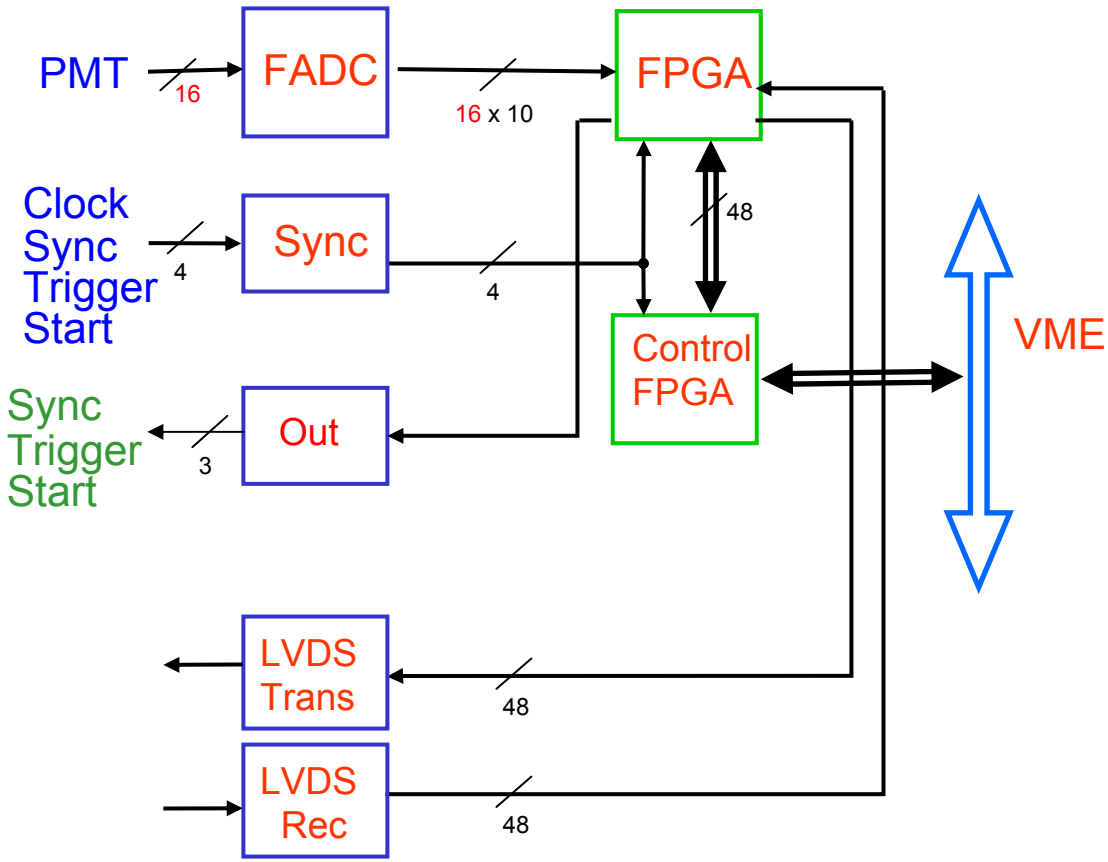
- The reconstructed-generated times are within the 10 ns tolerance even in presence of unacceptable noise



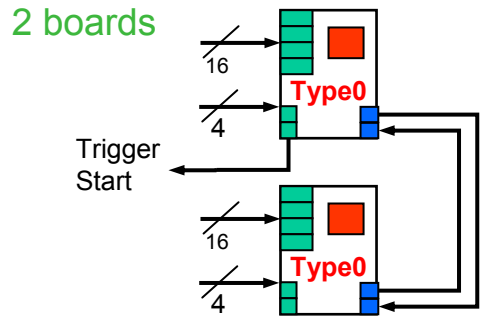
Present status

- Prototype board: Type0
  - Modified Type1 to check the connectivity with the Type2
- Selected components
  - Main FPGA XCV812E-8-FG900 and XCV18V04 config. ROM
    - larger than the strictly needed size
  - Interface and control FPGA XCV50E-8-FG256 and XCV17V01 config. ROM
  - ADC AD9218 (dual 10 bits 100 MHz)
  - Clock distribution CY7B993V (DLL multi-phase clock buffer)
  - LVDS serializer DS90CR483 / 484 (48 bits - 100 MHz - 5.1 Gbits/s)
  - LVDS connectors 3M Mini-D-Ribbon
- FPGA design
  - Design (by means of Foundation) and simulation of the model for the LXe is completed
  - VHDL parameterization (including timing) is ready

Prototype board : Type 0



- VME 6U
- A-to-D Conversion
- Trigger
- I/O
  - 16 PMT signals
  - 2 LVDS transmitters
  - 4 in/2 out control signals
- Complete system test



- Board Design
  - Almost ready: under simulation
  - Implementation by means of CADENCE
  - Board routing

- Tentative time profile
  - Prototype board ready in **April**
  - Final design ready by **autumn 2003**
  - Mass production may start by the **end of 2003** or **beginning 2004**
  - Estimated production, test and integration time **1 year**

Detailed functional description

First layer: Type1 Boards

LXe inner face

Each board:

- receive 16 PMT analog signals
- digitize the waveforms
- equalize the PMT gains
- subtract the pedestals
- compute the Q-sum
- find the PMT with max charge
- compute the min. arrival time
- store waveforms in FIFO
- send data to the next board

LXe lateral and outer faces

Each board:

- receive 16 PMT analog signals
- digitize the waveforms
- equalize the PMT gains
- subtract the pedestals
- compute the Q-sum
- store waveforms in FIFO
- send data to the next board

First layer: Type1 Boards

Timing counters

Each board:

- receive 16 PMT analog signals
- digitize the waveforms
- equalize the PMT gains
- subtract the pedestals
- find hit clusters
- compute the Q-sum
- (compute the Z position)
- find the PMT with max charge
- compute the arrival time
- store waveforms in FIFO
- send data to the next board

Second layer: Type2 Boards

LXe inner face

Each board:

- receives data from 10 type1
- computes the Q-sum
- equalizes the faces
- find the PMT with max charge
- computes the min arrival time
- sends data to the next board

LXe lateral and outer faces

Each board:

- receives data from 10 type1
- computes the Q-sum
- equalizes the faces
- sends data to the next board

Second layer: Type2 Boards

Timing counter

Each board:

- receives data from 6 type1
- propagate hit-cluster
- find the relevant hits
- computes the arrival time
- sends data to the final board

Final layer : Type2 Board

The board
- receives data from type-2 boards
- computes E_γ , Θ and Φ
- computes the γ arrival time
- computes Θ and Φ for the positron
- computes the Positron arrival time

generates triggers

- Normal acquisition trigger
  - makes use of all variables of the photons and the positrons with baseline algorithms
- Debugging triggers
  - generated by relaxing 1 or 2 selection criteria at the time for a fraction of normal triggers
- Calibration triggers
  - connection of auxiliary external devices (calorimeters) through further Type1 boards
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Details of the Trigger System

- Flexibility
  - the present trigger algorithms could not be the final ones
  - LXe and Timing Counters have different algorithms
- Standard (VME 6U and 9U)
  - limited data flow through the bus
  - standard commercially exploitable
  - front panel space and reduced number of stages
- FADC Frequency (100 MHz)
  - compromise between accuracy & cost
  - many other electronic components can run at 100 MHz
- Dynamic Range
  - 10 bit FADC are available and adequate

- Board synchronization
  - events are uniformly distributed in time
  - the event time is a basic trigger variable

    synchronous operation of the trigger system
    - external clock distribution and PLL components
    - synchronization signal after each L2 trigger
- Interconnections
  - LVDS up to 5Gbits/s on 9 differential couples are available
    - reduced front panel space
    - reduced amount of cables
  - large latency : tran. (1.5*T+4.9) rec. (3.5*T+4.4) cable (10) = Tot (7*T)
- Minimal different types of boards (2 Types)
  - Type 1 : analog to digital conversion
  - Type 2 : pure digital
  - arranged in a tree structure
- Possible other uses
  - acquisition board for the tracking chambers

- 4 to 1 fan-in of Liquid Xe lateral faces
  - these are relevant only for Q_{tot}
  - a 1 to 1 solution would require a further structure layer
- Total trigger latency
  - obvious impact on the amount of delay lines or analog pipelines
    - 4.5 periods in the FADC
    - 6 periods in the A to D board Type1
    - 7 periods for the interconnections
    - 4 periods in the first Type2 board
    - 7 periods for the interconnections
    - 6 periods in the final Type2 board

    ~ 350 ns delay
- System complexity
  - only two board types, but with eight different FPGA configurations
    - 3 different Type1
    - 4 different Type2