ILDハドロンカロリメータ検出層宇宙線試験装置の開発

Development of Cosmic-ray Test Stand for ILD HCAL

日本物理学会

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宇都宮大学峰キャンパス

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Outline

- Background/Motivation
  - ILC, ILD and AHCAL
  - Cosmic-ray test stand
- Research/Development
  - Verification
  - Synchronization of DAQ
- Prospects/Summary

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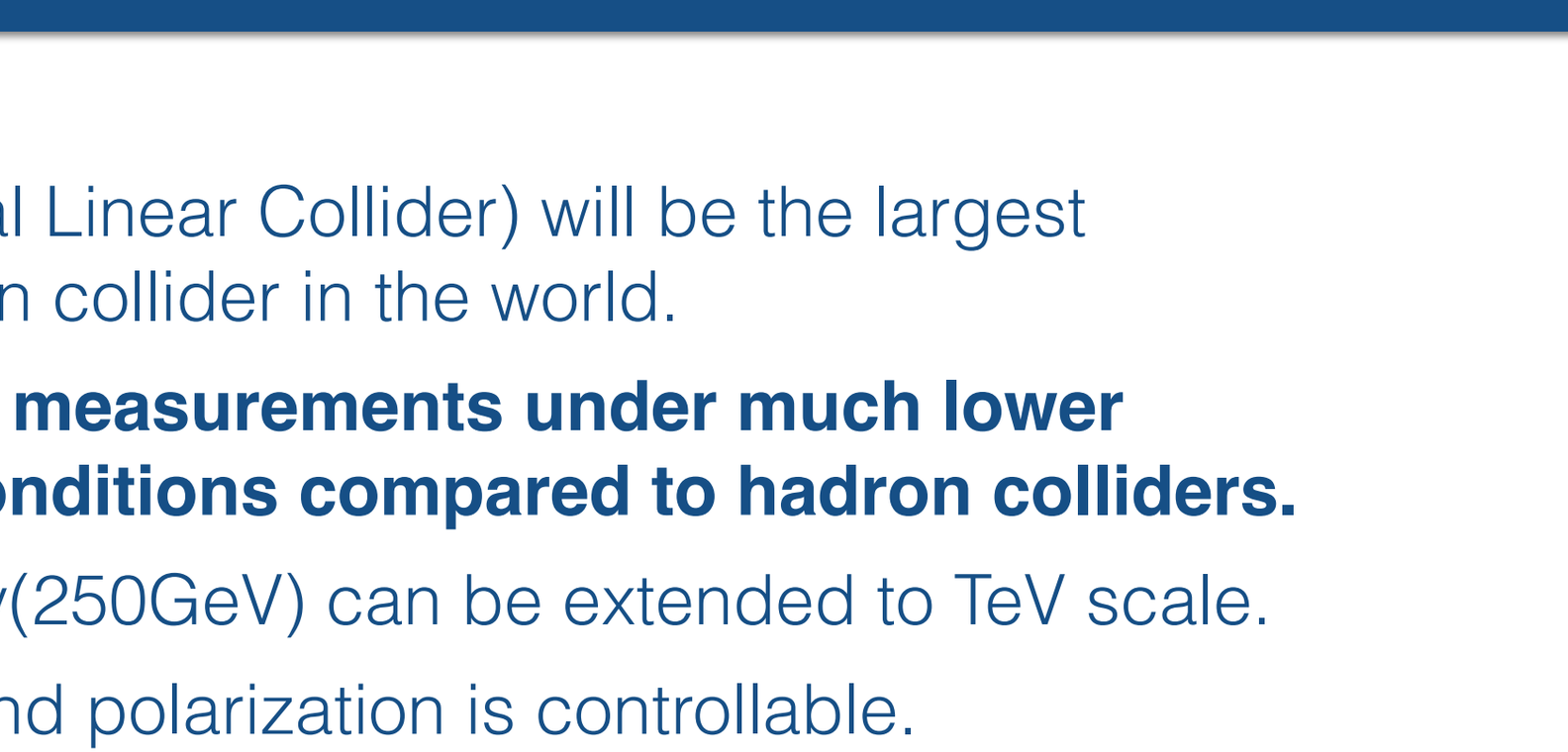
ILC Project

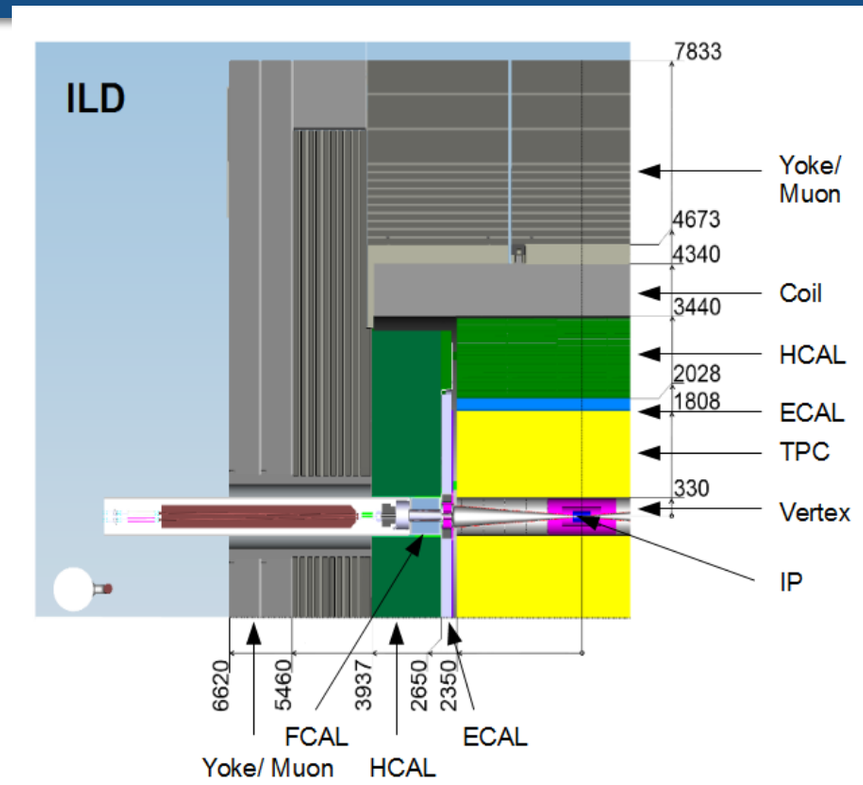
- ILC(International Linear Collider) will be the largest electron-positron collider in the world.
- **High precision measurements under much lower background conditions compared to hadron colliders.**
- Collision energy(250GeV) can be extended to TeV scale.
- Beam energy and polarization is controllable.
- Precise measurement on Higgs, Top at the ILC will play an important role to study new physics.



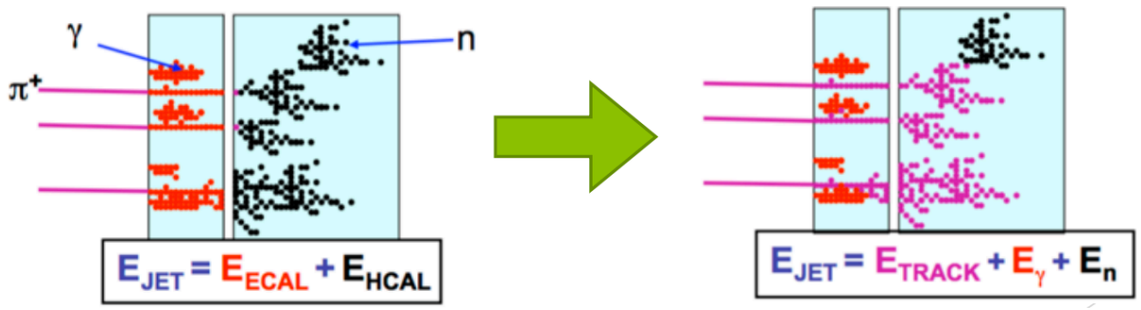
ILC Design

ILD and PFA

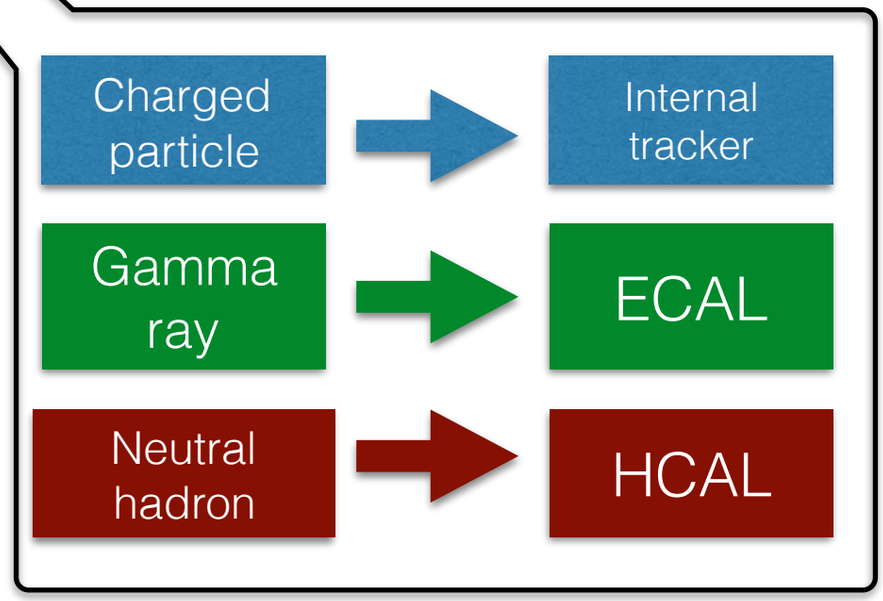
- ILD(International Large Detector), which is a strong candidate of the ILC detector, is designed on the basis of the PFA.
- **PFA(Particle Flow Algorithm)**
  - Events are reconstructed by identifying single particle in jet.
    - Energy of each kind of particles is measured by the most suitable detector.
    - PFA improves the resolution of jet energy.
- PFA requires **high granularity** calorimetry for both ECAL and HCAL.



ILD Design

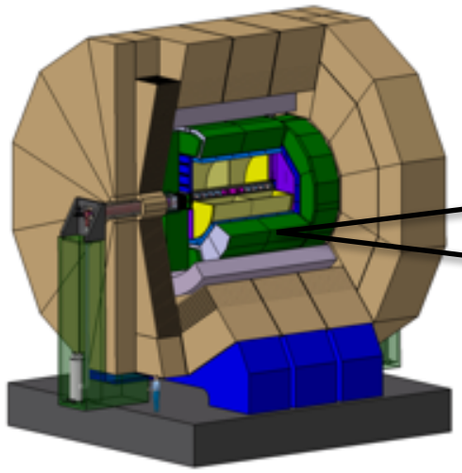


Energy reconstruction with PFA

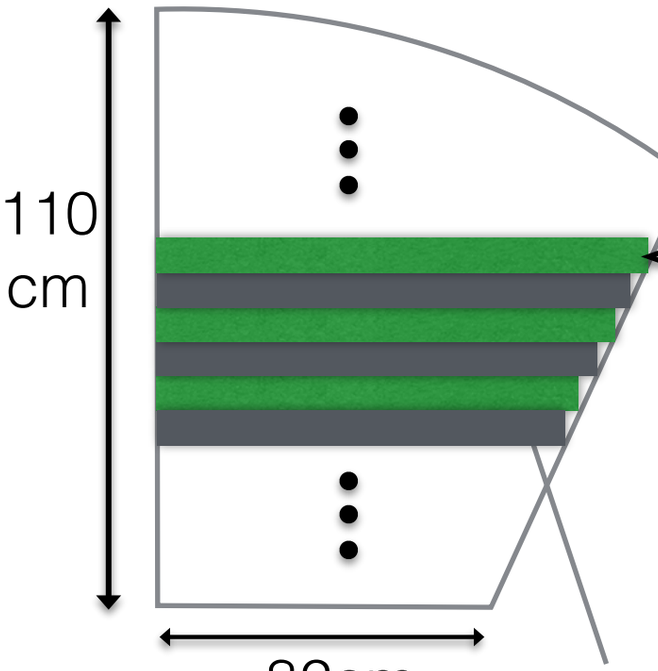


AHCAL Design

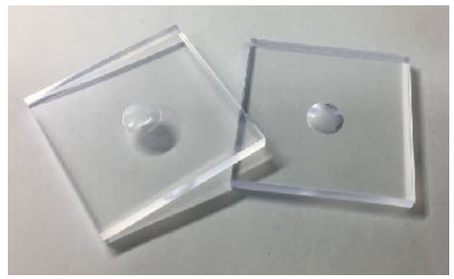
ILD Design



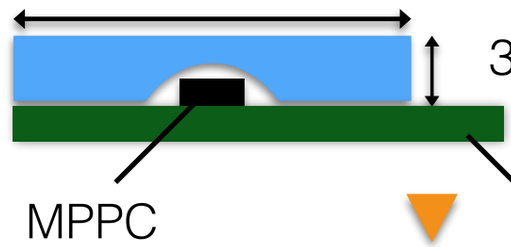
AHCAL module

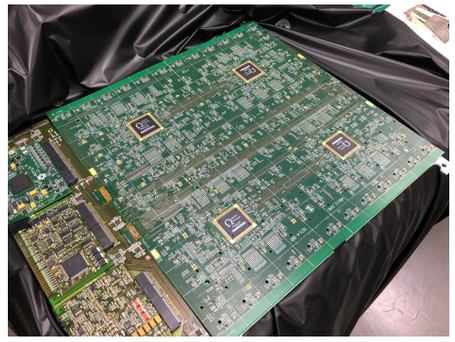


Active layer



Scintillator tiles





# of AHCAL modules (in barrel part):**32**

×

# of active layers:**48**

×

#of units/1 active layer:**18**
# of tiles/1 unit:**144**

~O(**10^6**)

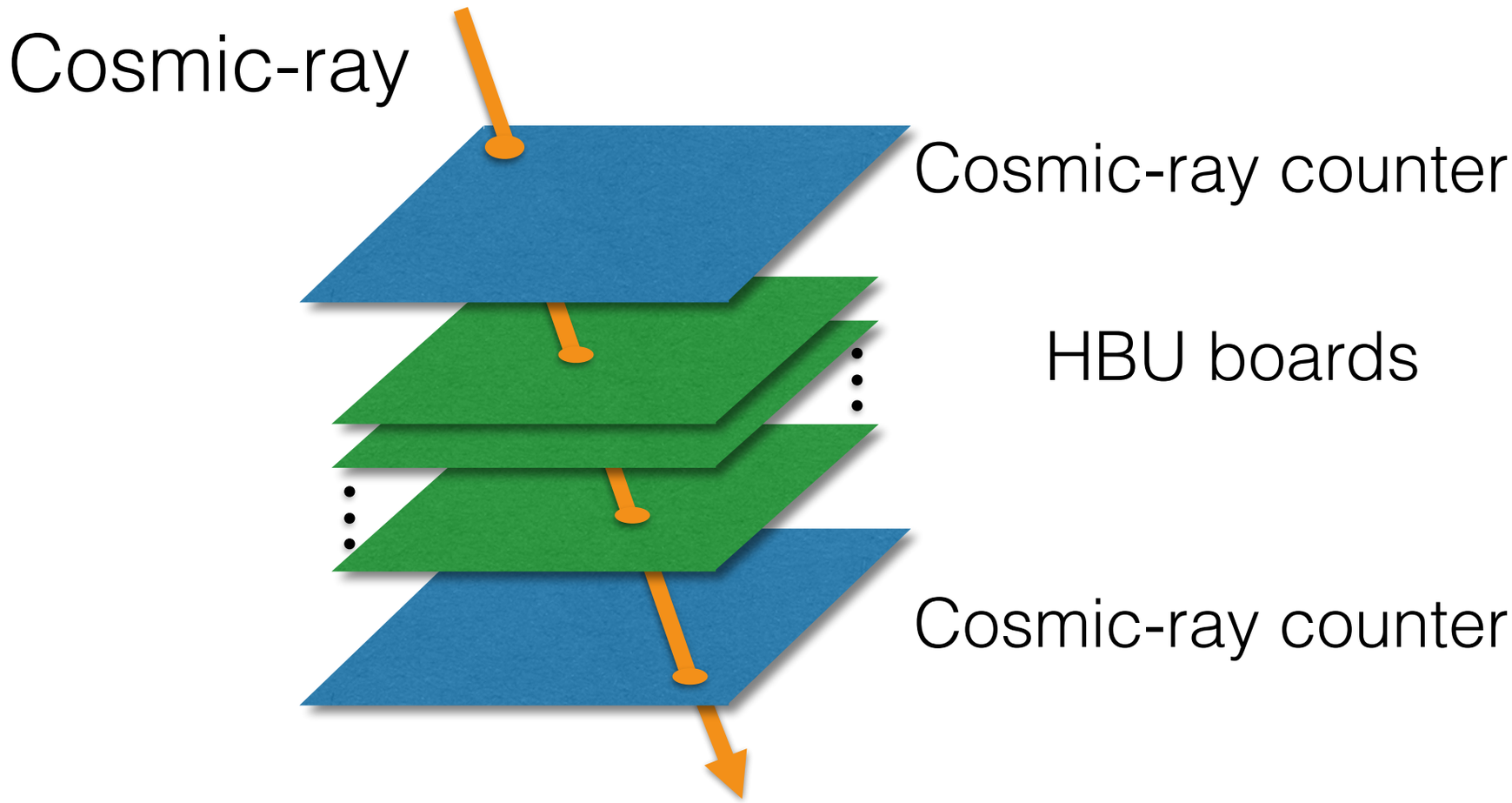
- In order to identify particles in a jet one by one, we have to use **many scintillator tiles and MPPCs**.

AHCAL Large Prototype

- A large prototype is now under construction in DESY.
- This prototype consists of 40 layers of 2×2 HBUs with 576 tiles
  - This prototype is **scalable to full AHCAL.**
  - **24k~27k tiles** are mounted in total.
- The motivation is:
  - prove mass productivity
  - investigate response to hadron shower
  - operate fully integrated system
- Beam test with hadrons at CERN SPS is planned in 2018.

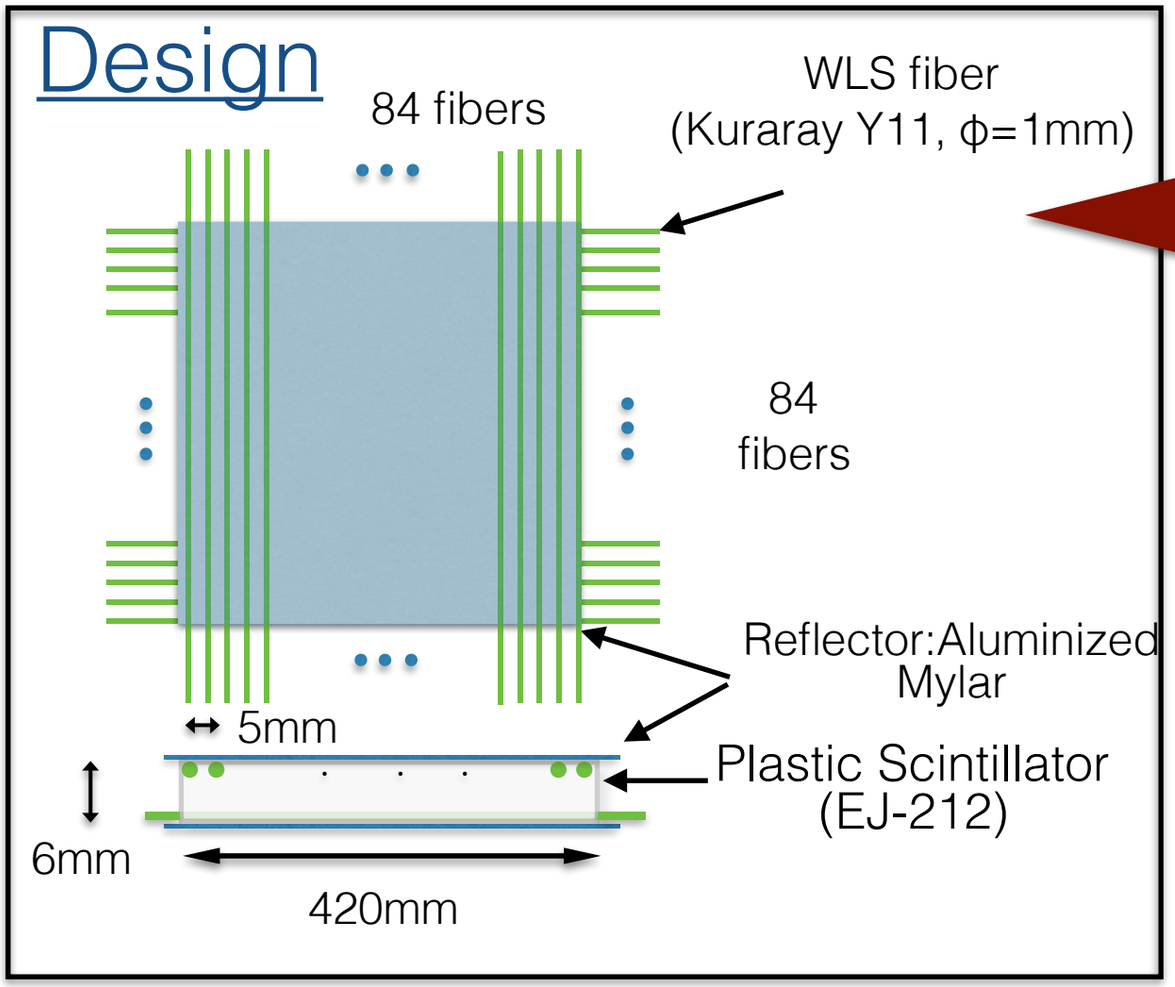
EUDET steel stack

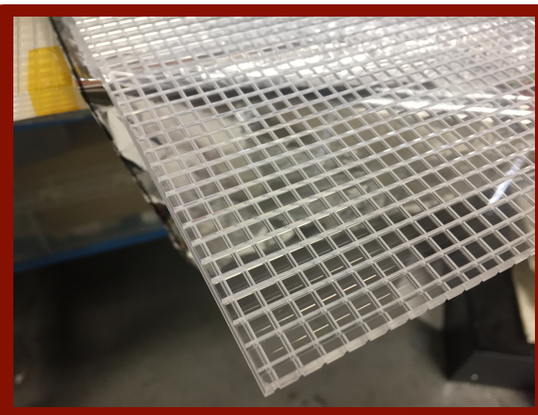
Calibration with Cosmic-ray



- Mass calibration with cosmic-ray is a good method in terms of **cost and easiness**.
- By measuring the trajectory at high precision with two counters, we can know the **hit position in the tile** and **the incident angle**.
- σ~5mm is enough as the position resolution.

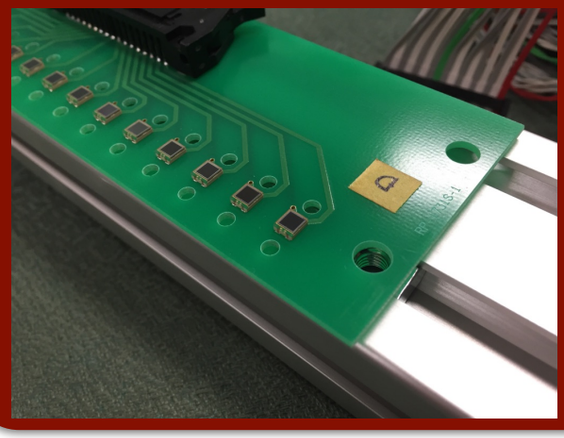
Counter Design





Scintillation photon is read out by WLS fibers

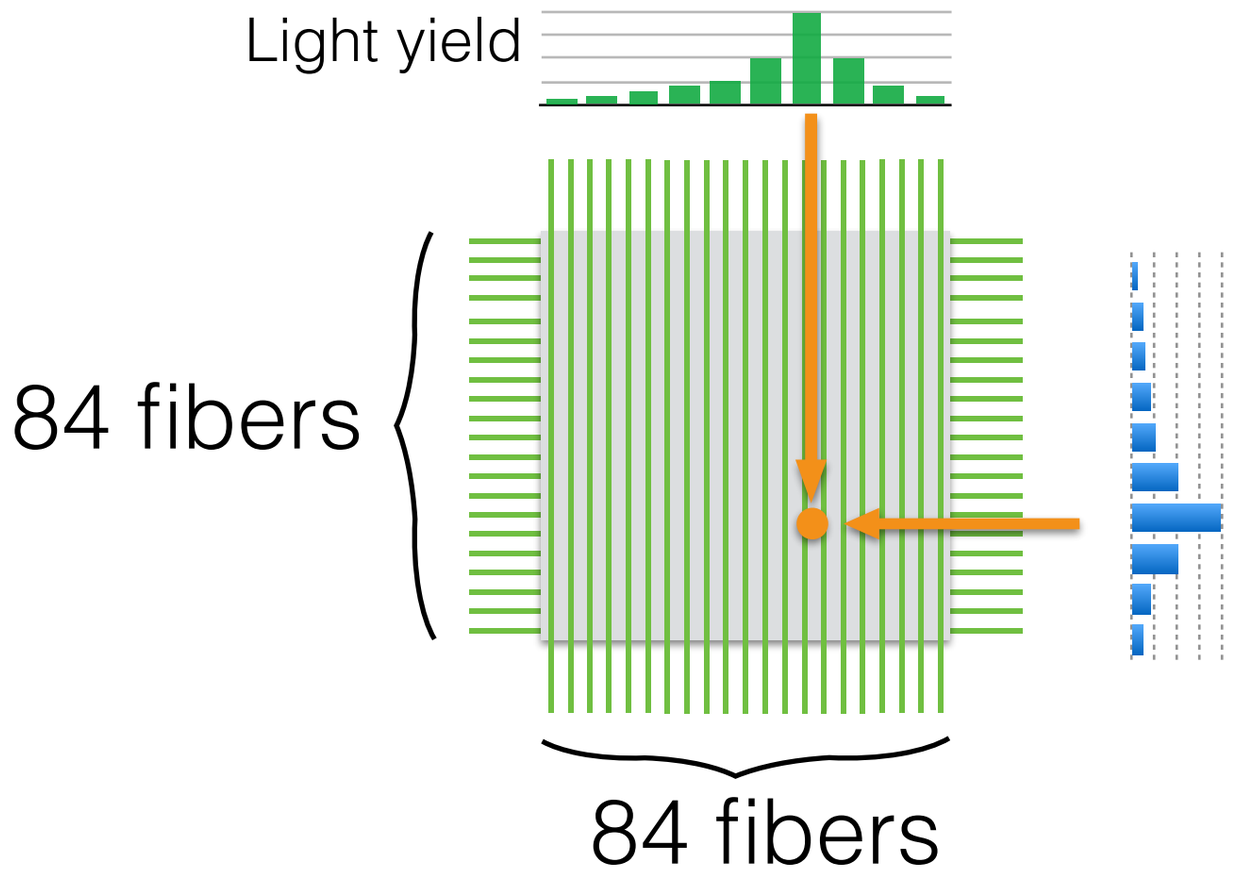
Grooves at 5mm interval



WLS fiber and MPPC are aligned on PCB

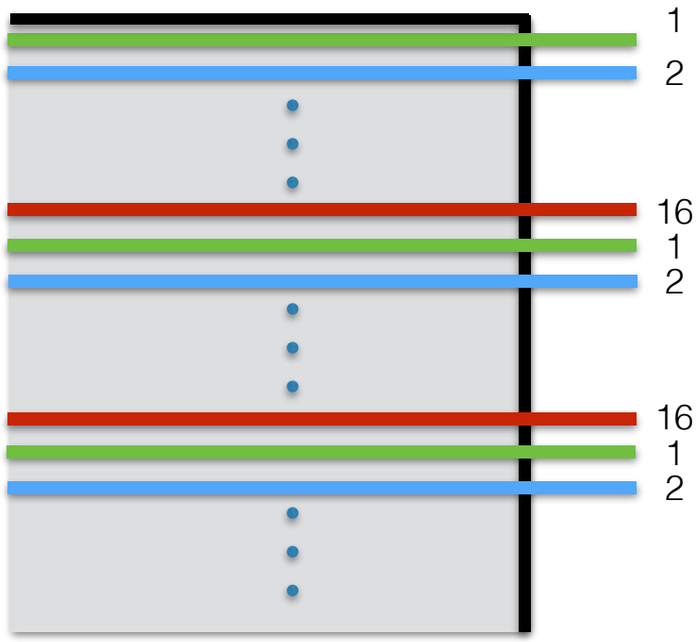
- Scintillation light is read out by WLS fiber with MPPCs at both ends.
- 84 grooves to embed WLS fibers are arranged at 5mm intervals on both sides of the scintillator plate.
- Grooves on both sides are orthogonal to each other to reconstruct 2-D hit position.

Counter Idea

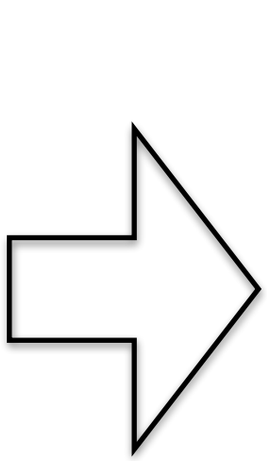


- We can obtain 2-D light yield distribution.
- **By use of the center of light yield distribution, the hit position is reconstructed on event-by-event basis.**
- 336 channels are required if all fibers are read out individually.

Reduction of Readout Channels



84 fibers



MPPC1

MPPC2

MPPC16

16 MPPC
S13360-3050PE
(Hamamatsu HPK)

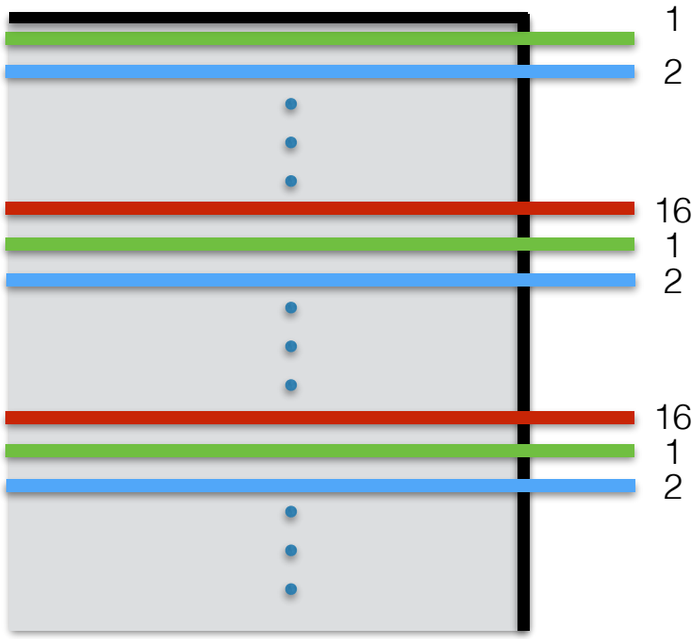
CONCEPT

Bundle terminal

five or six fibers

- By bundling every 16 fibers periodically, we can reduce the number of readout channels by factor of five.
- There are fake hits due to the periodical light yield distribution.
  - Fake hits are eliminated with the hit position in the active layer.

Reduction of Readout Channels



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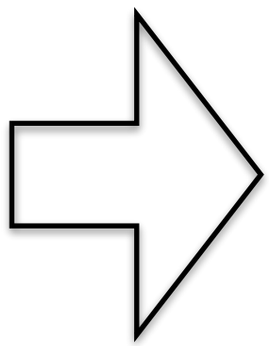
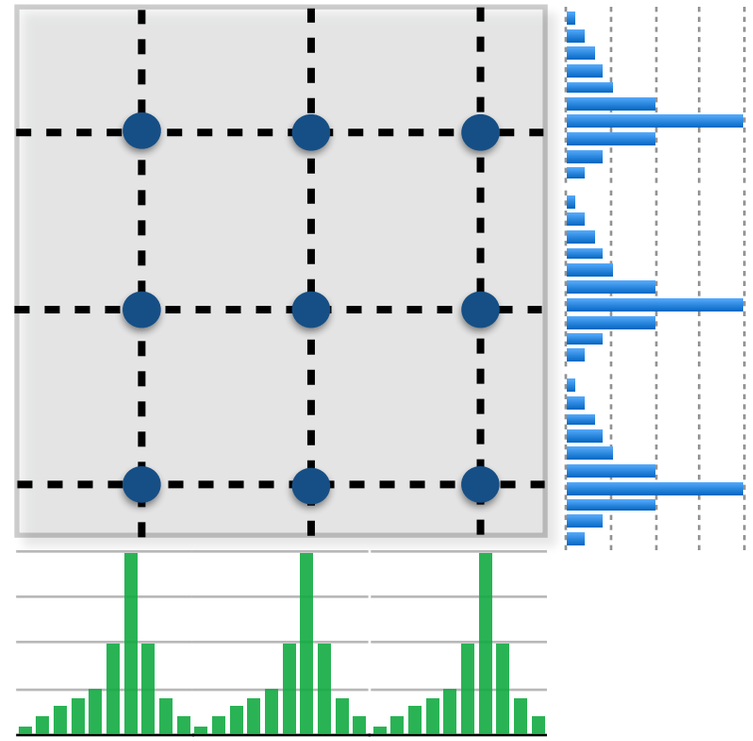


16 MPPC
S13360-3050PE
(Hamamatsu HPK)

CONCEPT

Ambiguity exists



Periodic distribution

- By bundling every 16 fibers periodically, we can reduce the number of readout channels by factor of five.
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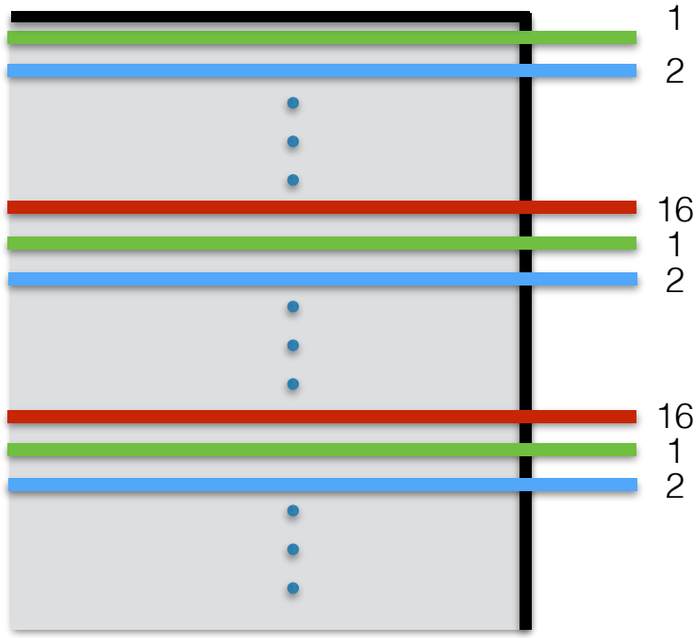
Reduction of Readout Channels



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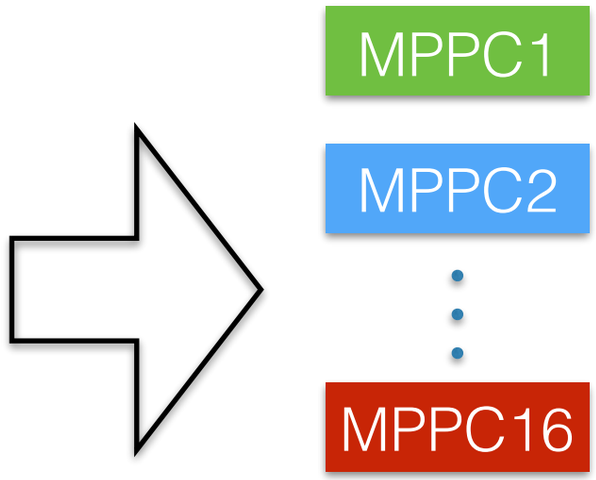

16 MPPC
S13360-3050PE
(Hamamatsu HPK)

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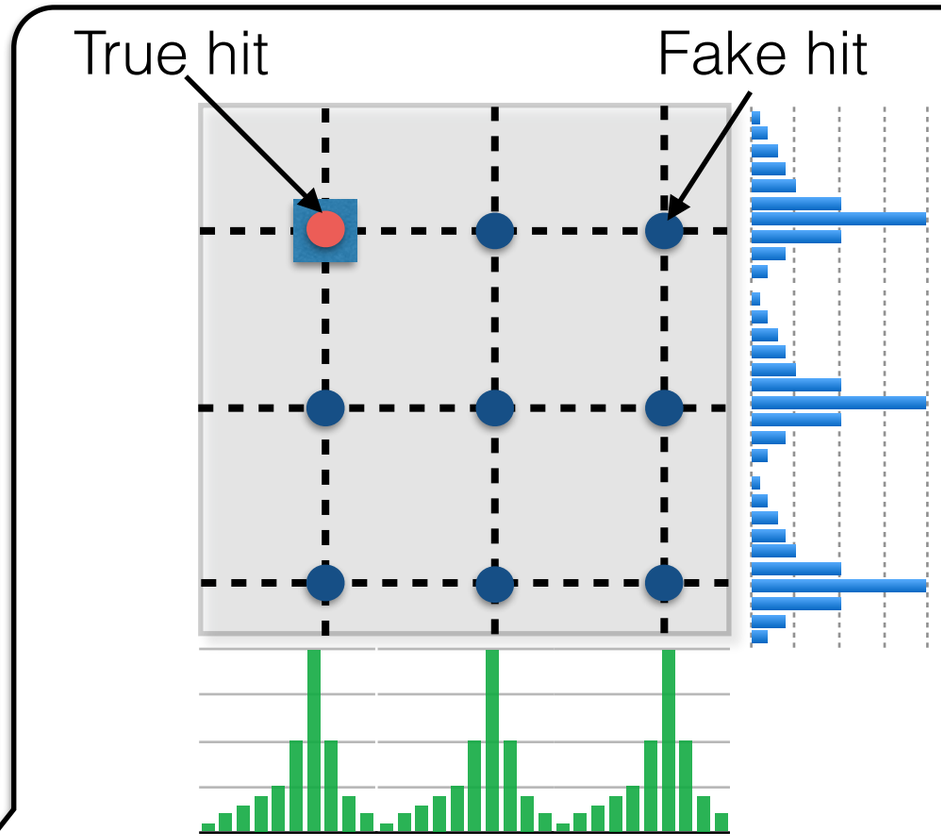

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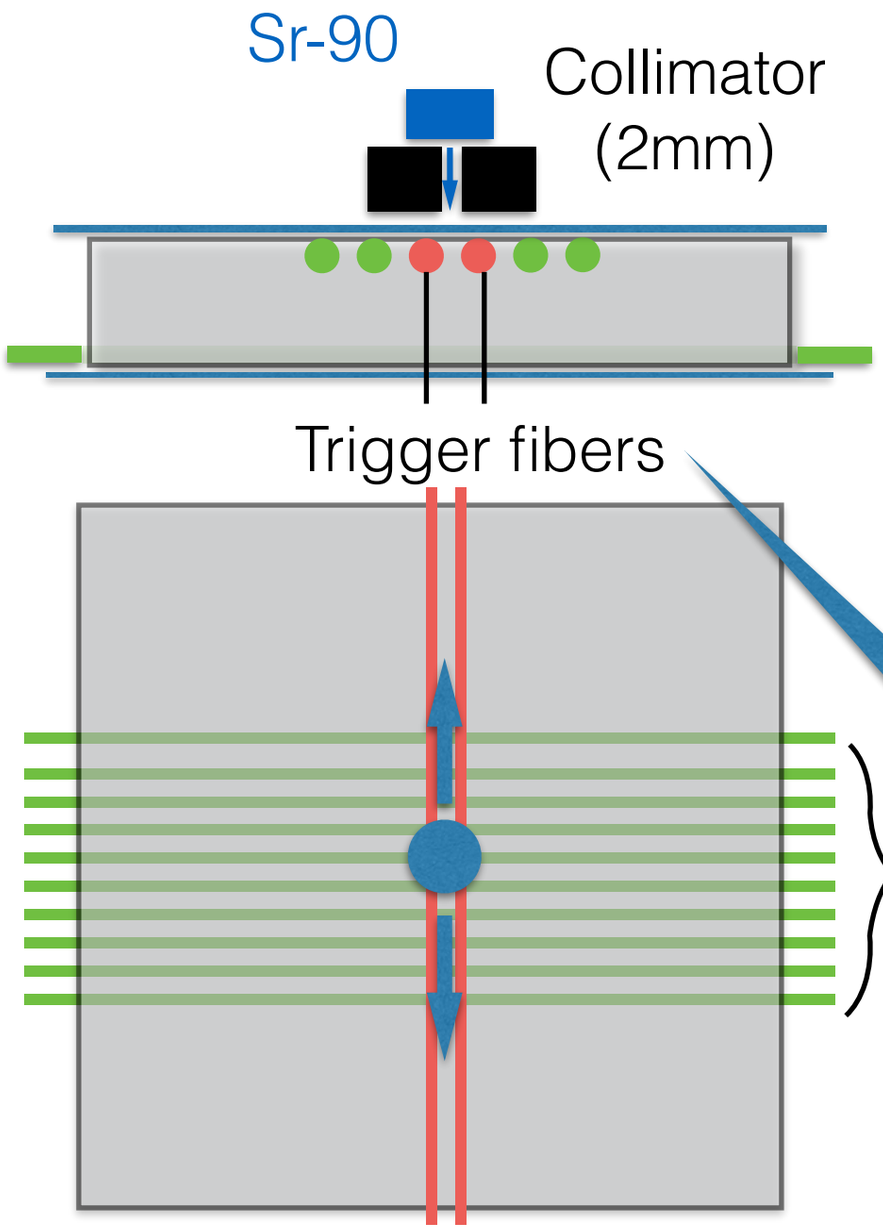
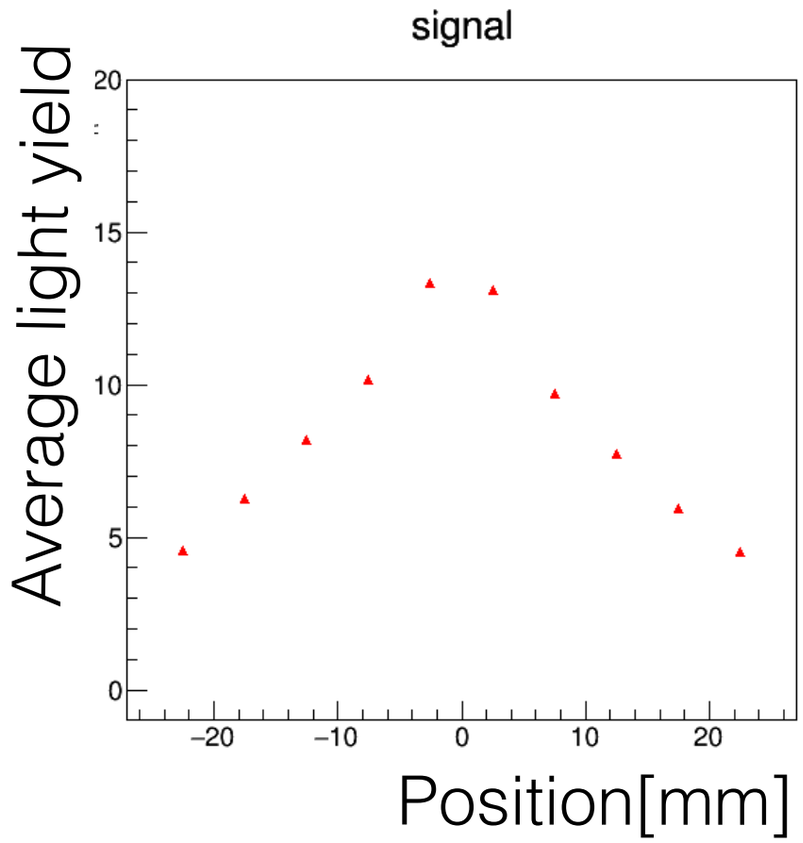
  - **Synchronization of DAQ**
- Prospects/Summary

Test of Position Reconstruction

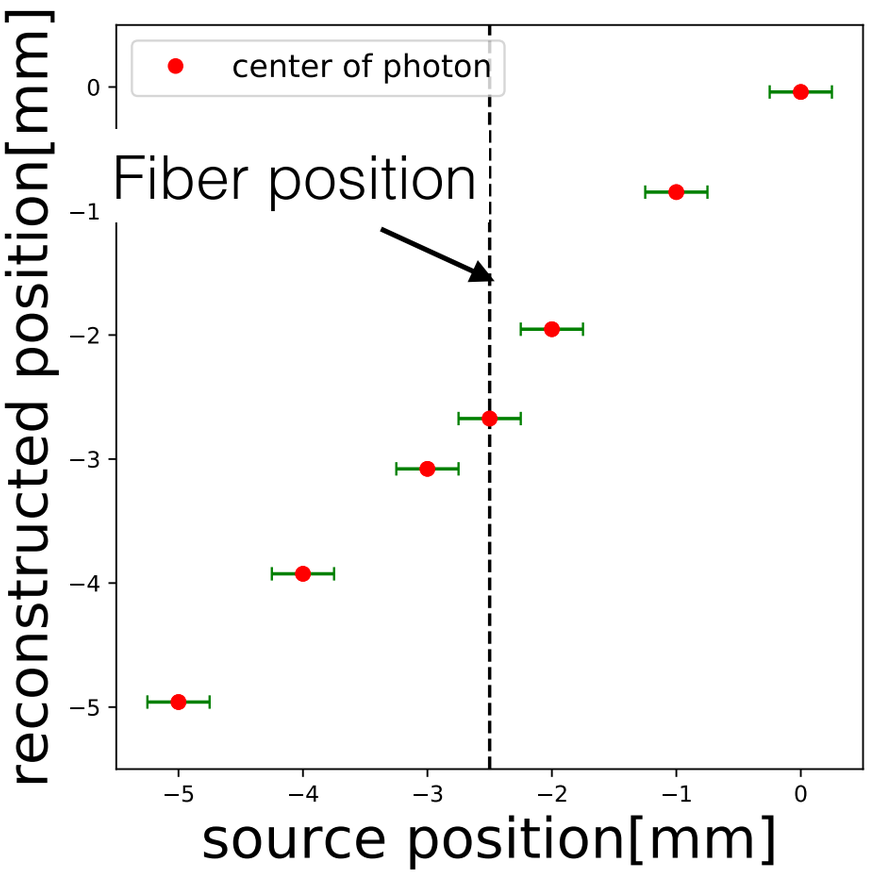


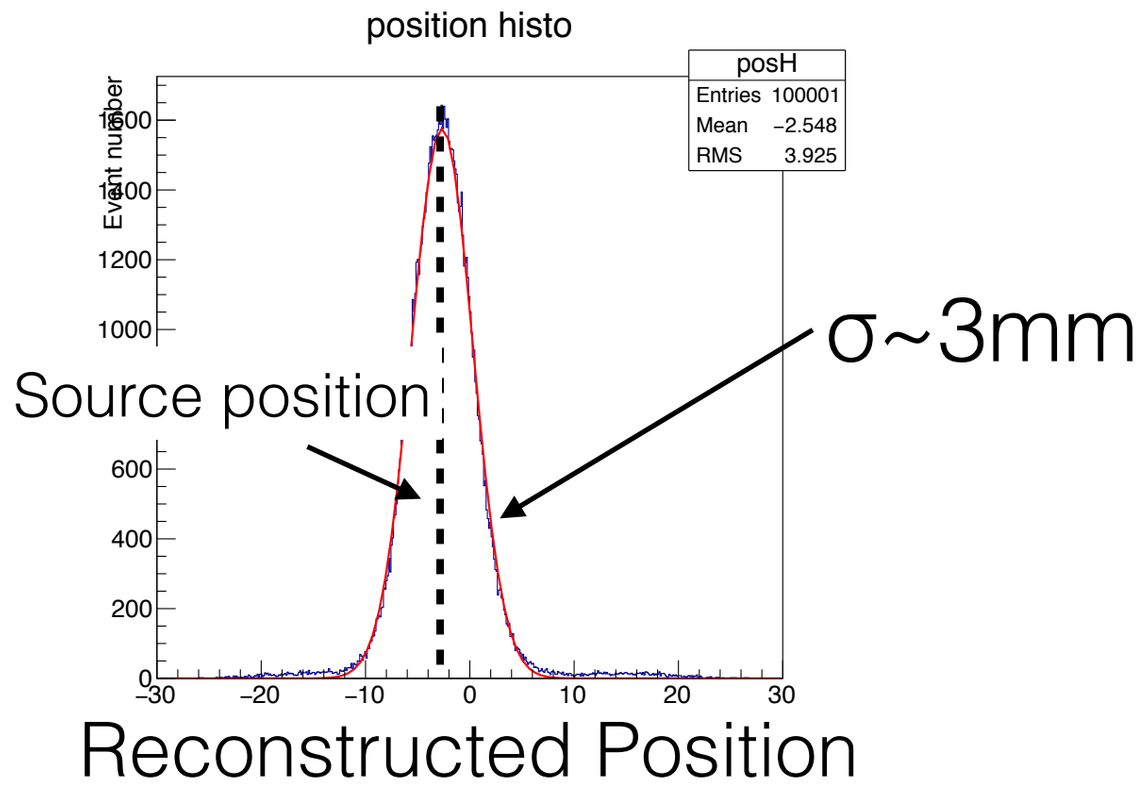


Events are triggered by
two fibers in the top face

Reconstruct the hit position
with **10** fibers in the bottom face

Verification Result



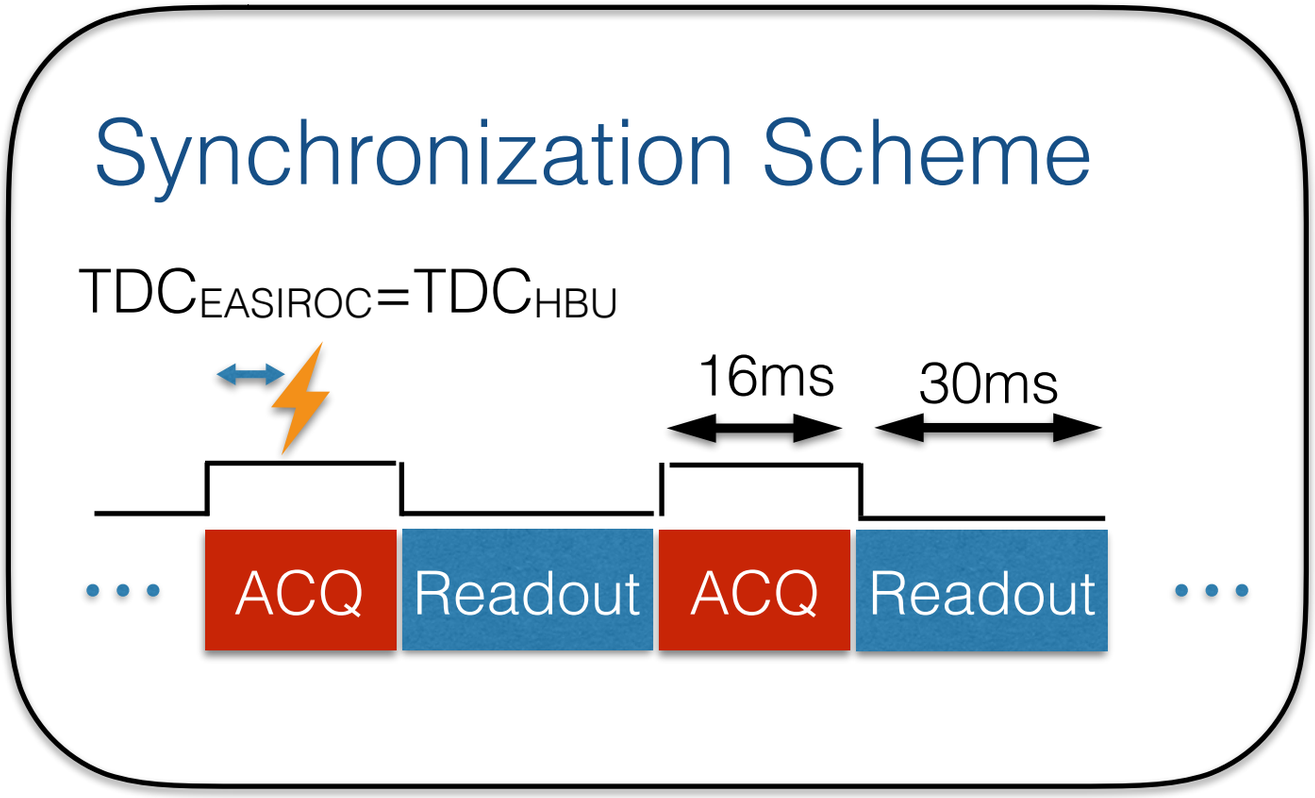


- With 10 fibers, the position resolution is about **σ~3mm.**
  - Correction due to limited number of fibers was necessary.
- A dedicated simulation shows that the resolution would slightly be worsened to **σ~4mm** by fiber bundling because of the wide light yield distribution.

We decided to bundle every 16 fibers

DAQ Synchronization

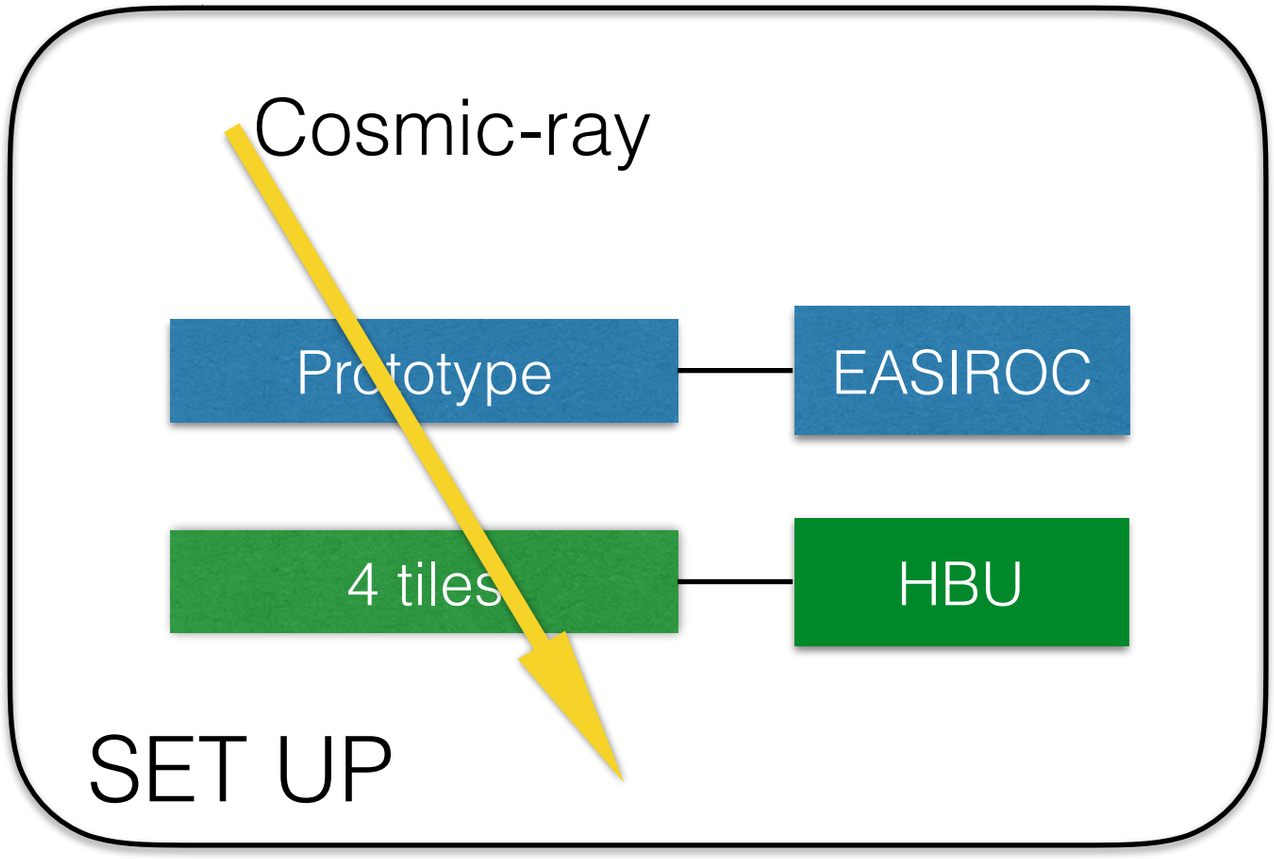
- The DAQ system of the HBU(AHCAL) is based on the timing scenario of the ILC or the test beam facility.
- In order to calibrate HBU with cosmic-ray, we should synchronize between different two DAQ systems:
  - EASIROC modules(for cosmic-ray counter) and HBU

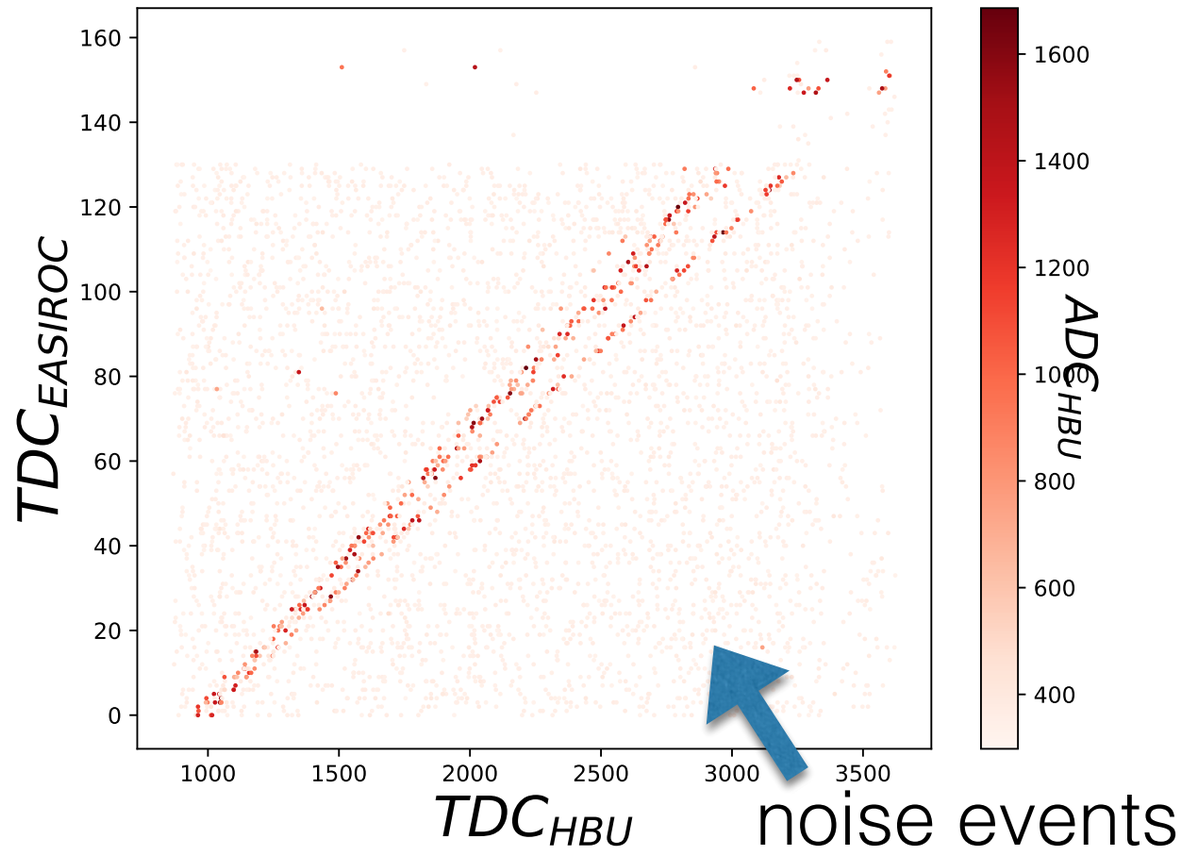


Basic concept:

1. Use the same clock(40MHz)
2. Count acquisition signal (ACQ) provided by HBU
3. Measure the hit time from the rising edge of ACQ

Confirmation of Synchronization

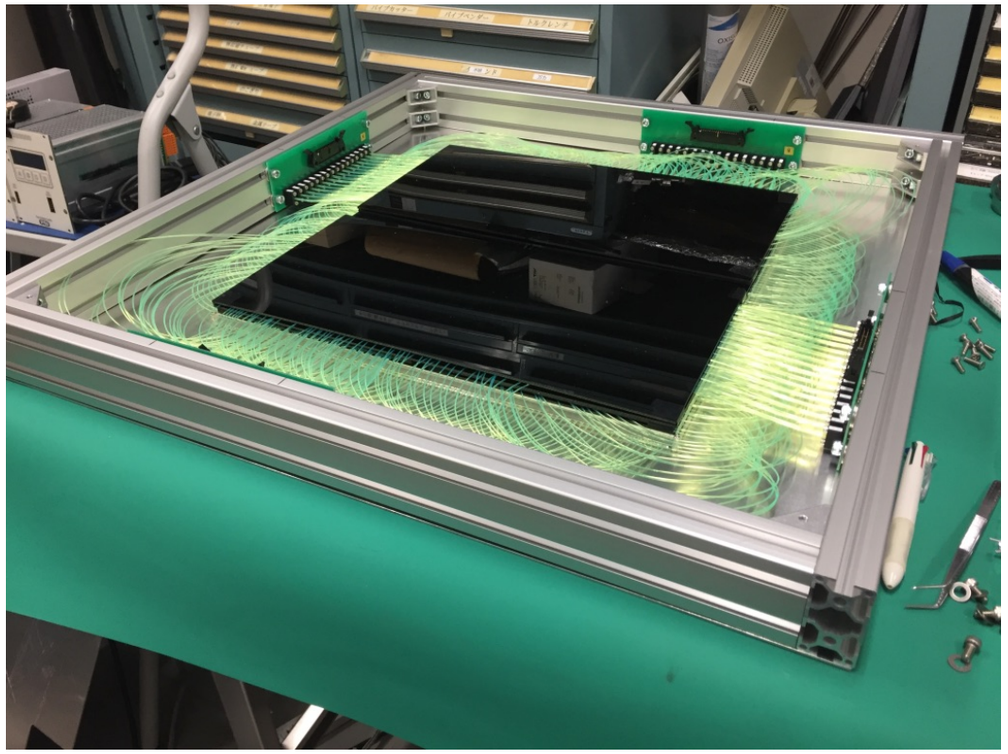




- We tested the synchronization between the two modules.
- Different slopes on the right graph correspond to different ASIC chip.
- Most of these events is supposed to come from cosmic ray: this shows that the **synchronization works successfully**.

Status and Prospect

- By use of the cosmic ray test stand, we will test multiple HBUs at DESY.
- Now construction of two counters is completed.
- We will bring our CR counters to DESY and start commissioning from the middle of October.
- Towards the commissioning, we are trying to calibrate the counter by radiation source.



▲ Construction has finished

Summary

- AHCAL's large prototype uses **a lot of scintillator tiles** so that it needs an easy way to calibrate them simultaneously.
- For HBU calibration with cosmic-ray, **we have developed a counter that can reconstruct 2-D hit position of cosmic-ray** on event-by-event basis.
- We succeeded the **synchronization between different DAQ systems**: EASIROC module and HBU.
- Since two counters have been constructed, now calibration on them is ongoing.
- We will start commissioning in the next month.

Thank you for listening!!

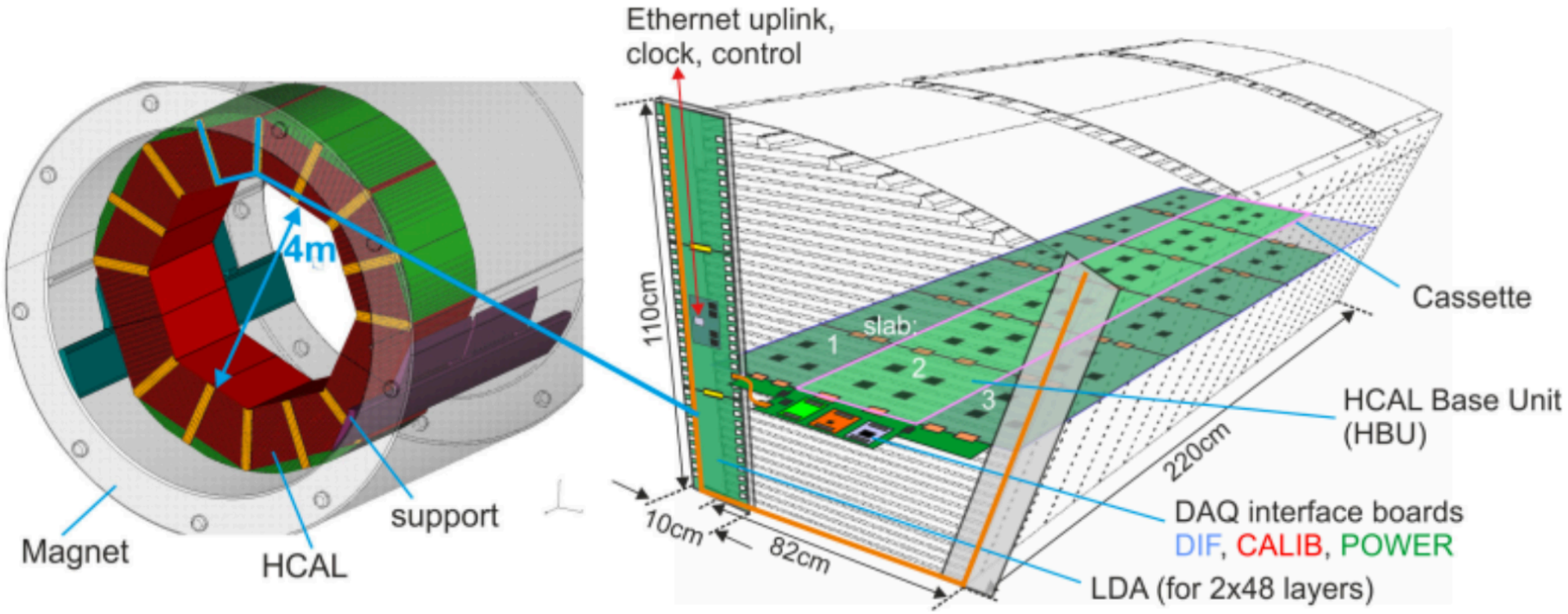
This research is performed with the help of
Masashi Yokoyama, Naruhiro Chikuma(The University of Tokyo)
Tohru Takeshita, Hisao Sato(Shinshu University)
Jiri Kvasnicka(DESY)

Back Up

Backup Index

- AHCAL structure
- Mainz test stand
- EASIROC module
- MPPC gain calibration
- Simulation for bundling
- DAQ diagram
- HBU TDC
- Interface integration(EUDAQ)

AHCAL Structure



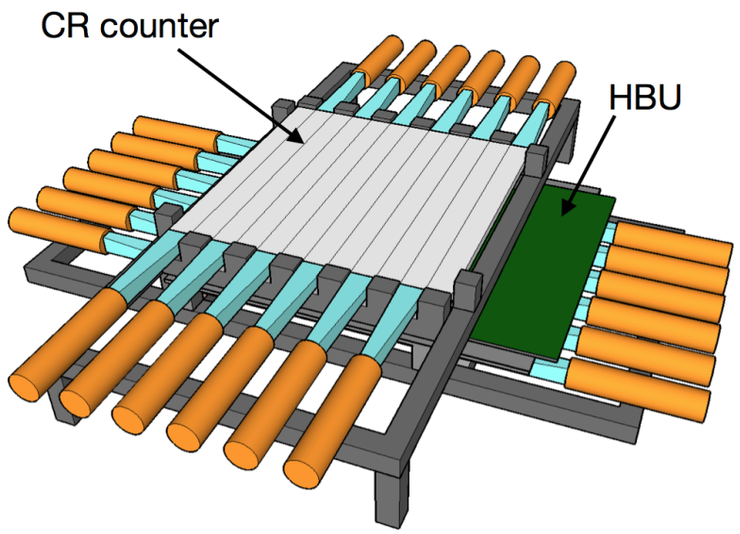
- HCAL in ILD consists of AHCAL modules.
- An AHCAL module consists of ~18 HBU(HCAL Base Unit)
- There are 144 scintillator tiles on one HBU.

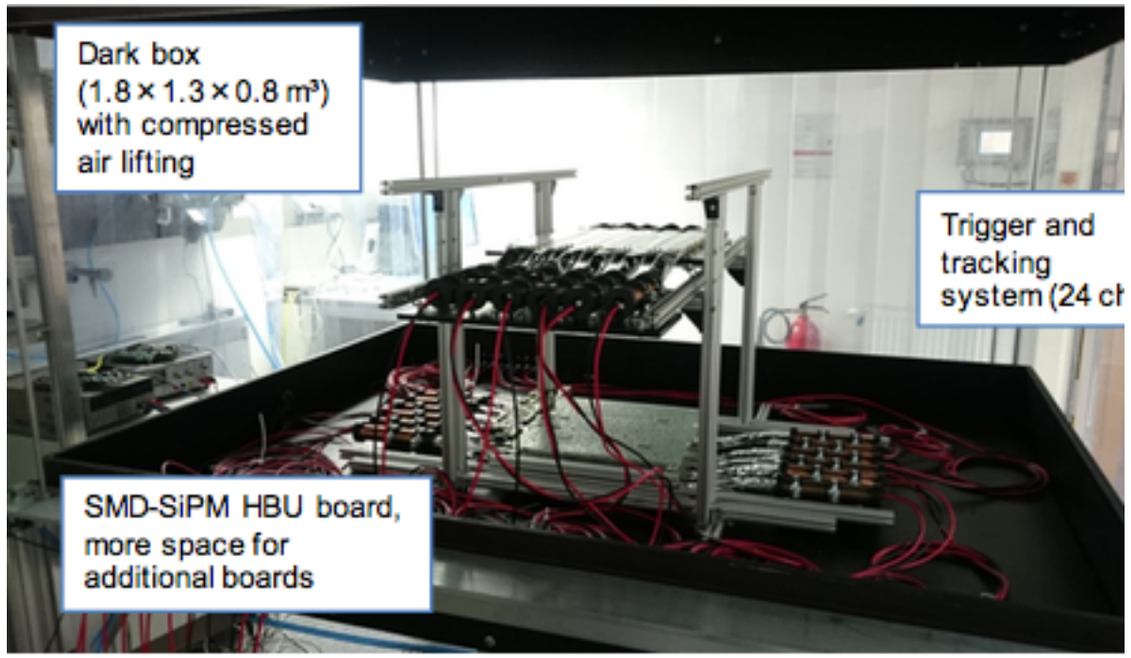
Mainz Test Stand

- A similar test stand is also developed at Mainz, but it is only used as a trigger counter.

Mainz CR test stand

- Scintillators on top and bottom of SMD HBU board to trigger cosmics
- Strip design for cost reduction
  - Each strip 36,5 x 3,015 cm²
- Components:
  - 24 PMTs
  - 24 ch. HV
  - 24 ch. VME discriminator
  - Dark box (1,8x1,3x0,8 m³)
  - FPGA for trigger logic, event validation, time stamping of triggered events





EASIROC Module

Discriminator

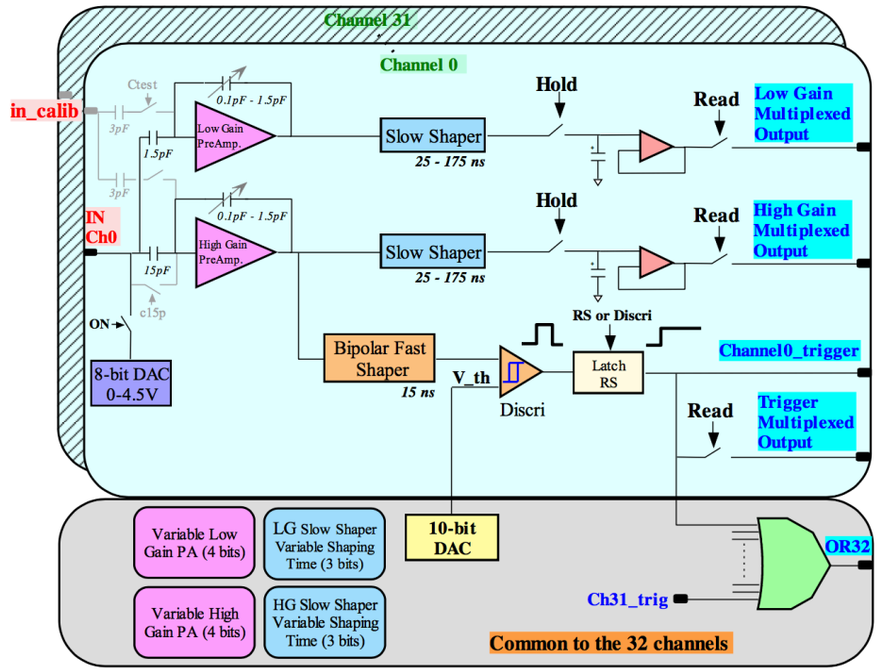
HV

ADC

Amp

DAC for adjusting HV

Shaper

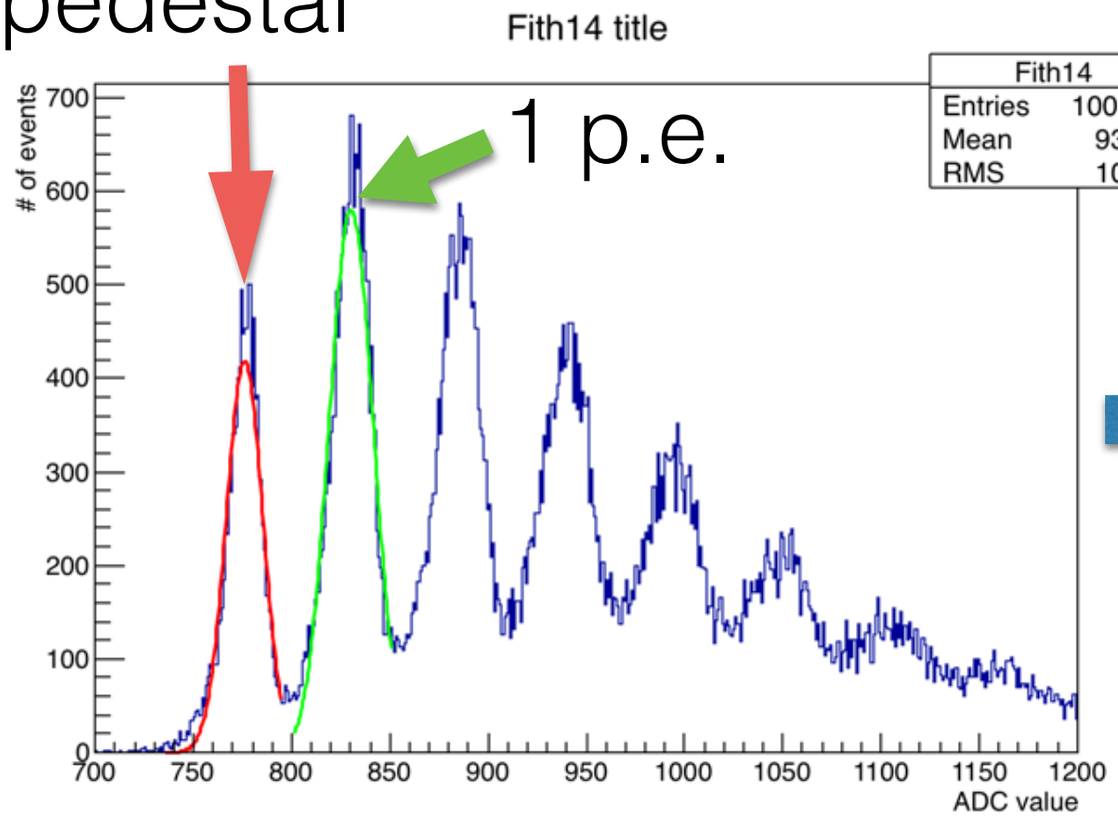


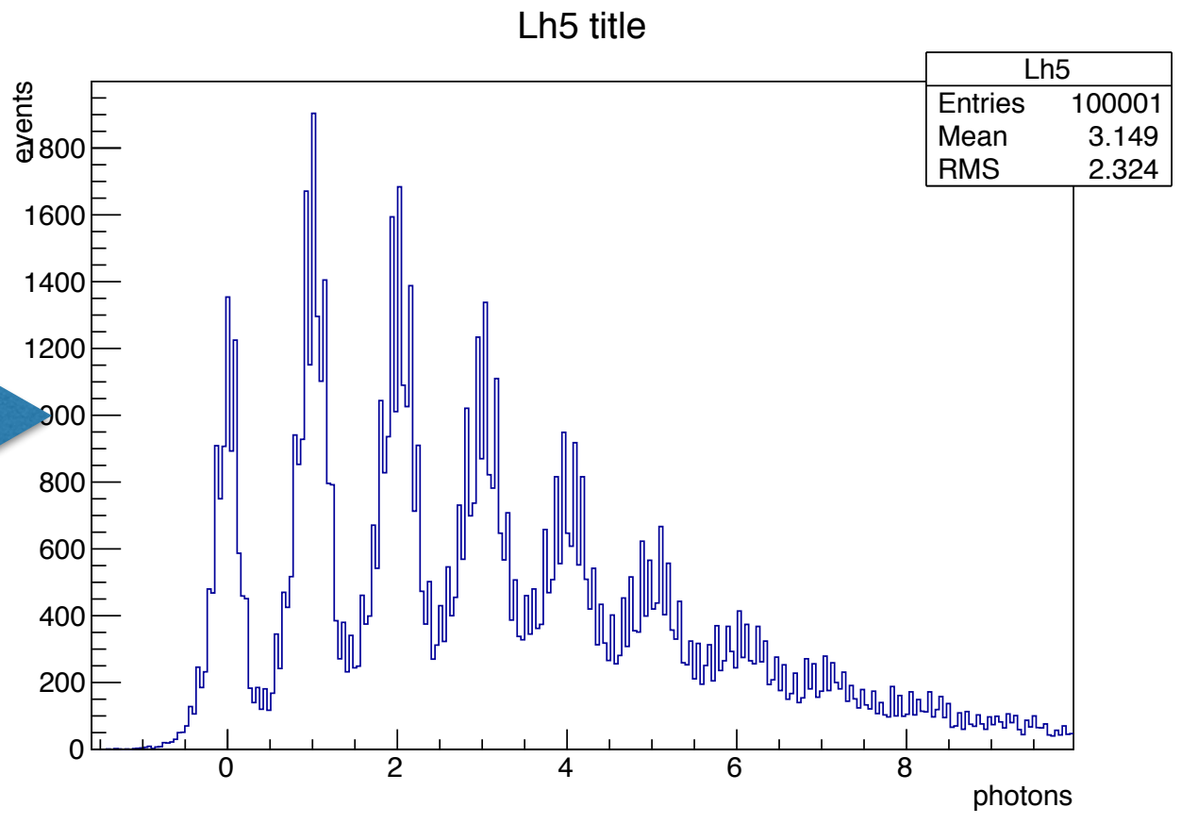
EASIROC circuit

- EASIROC module is a module for operation and data acquisition of multiple MPPCs.

MPPC Gain Calibration

pedestal



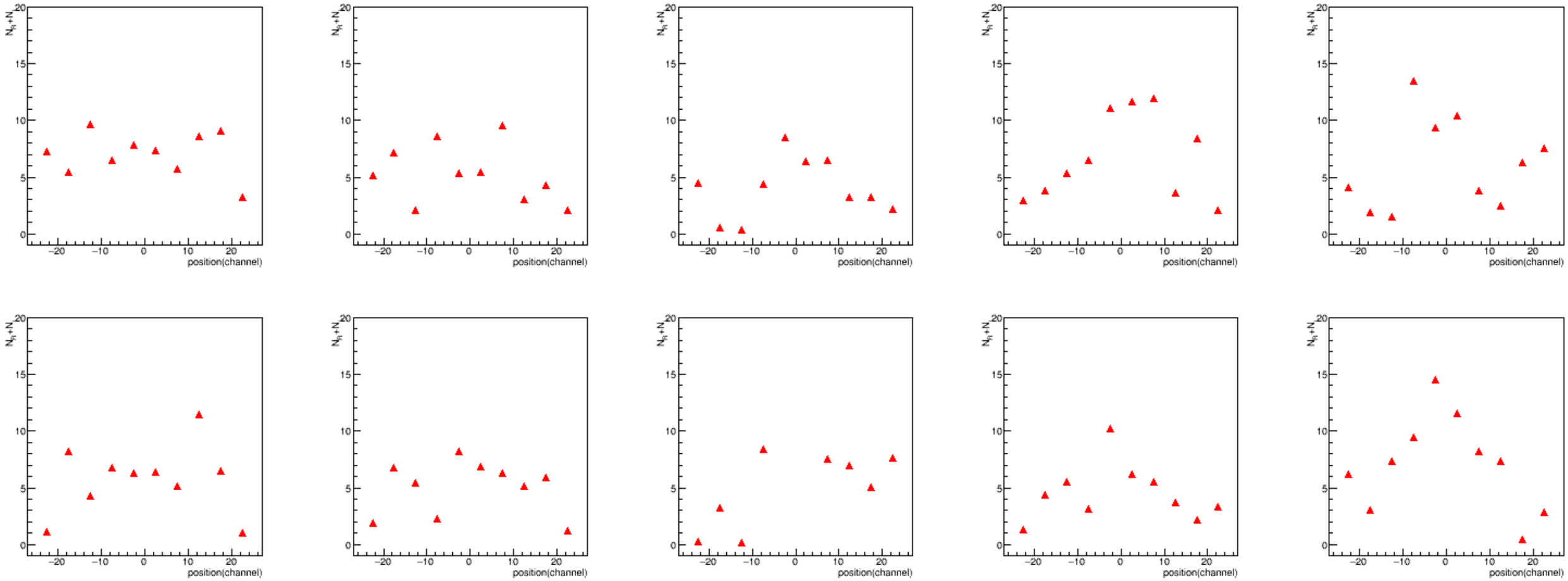


ADC histogram

Light yield histogram

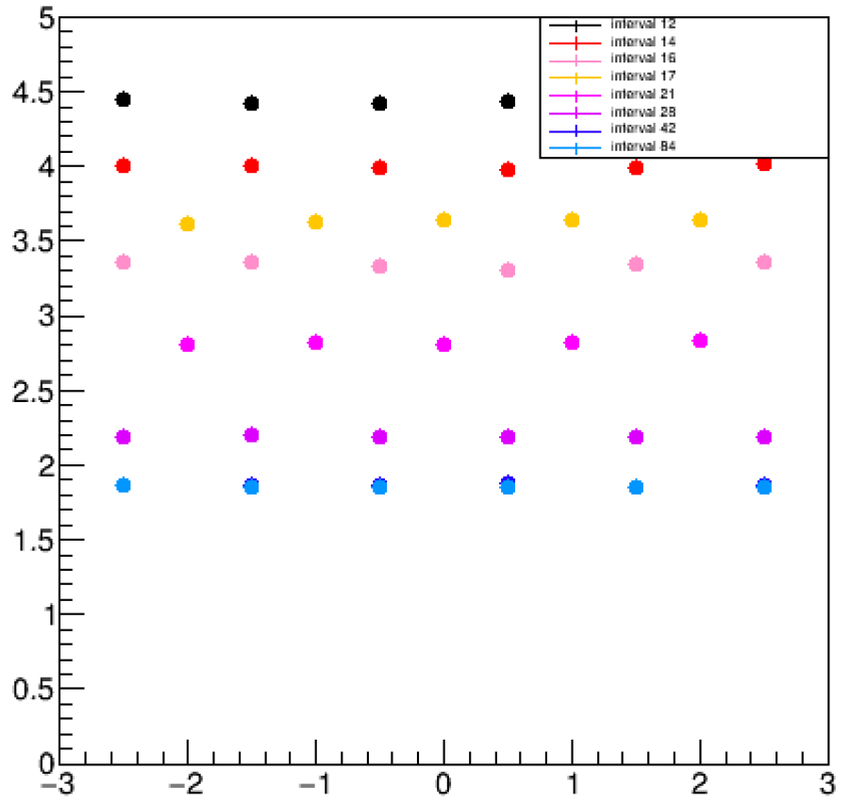
- By use of the EASIROC module, we can obtain the charge of multiple MPPCs on event-by-event basis.

First 10 Events when x_{rad} = 0mm



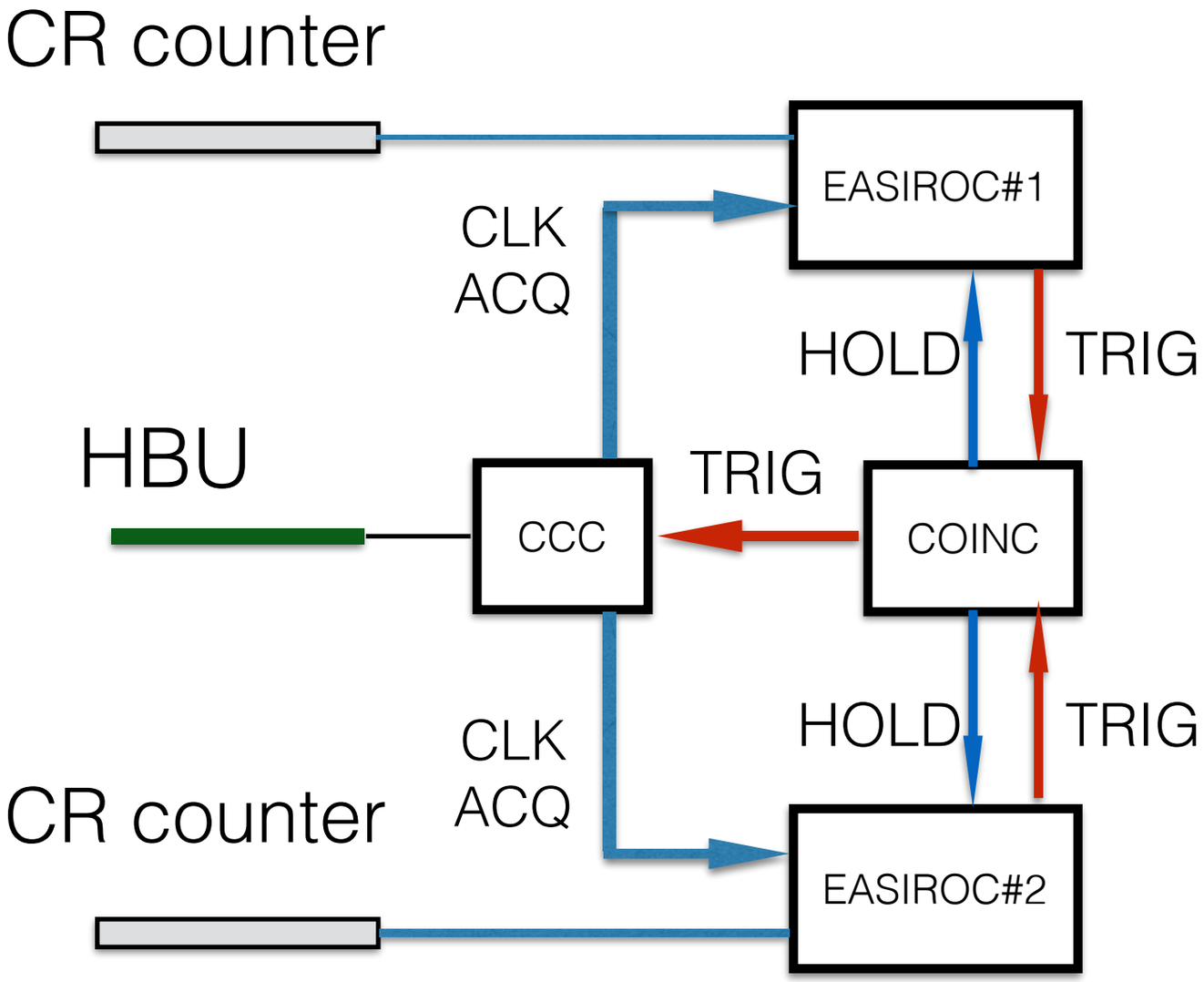
- Light yield of each fiber fluctuates largely, but we can calculate the true hit point by use of the center of light yield.

Simulation for Grouping



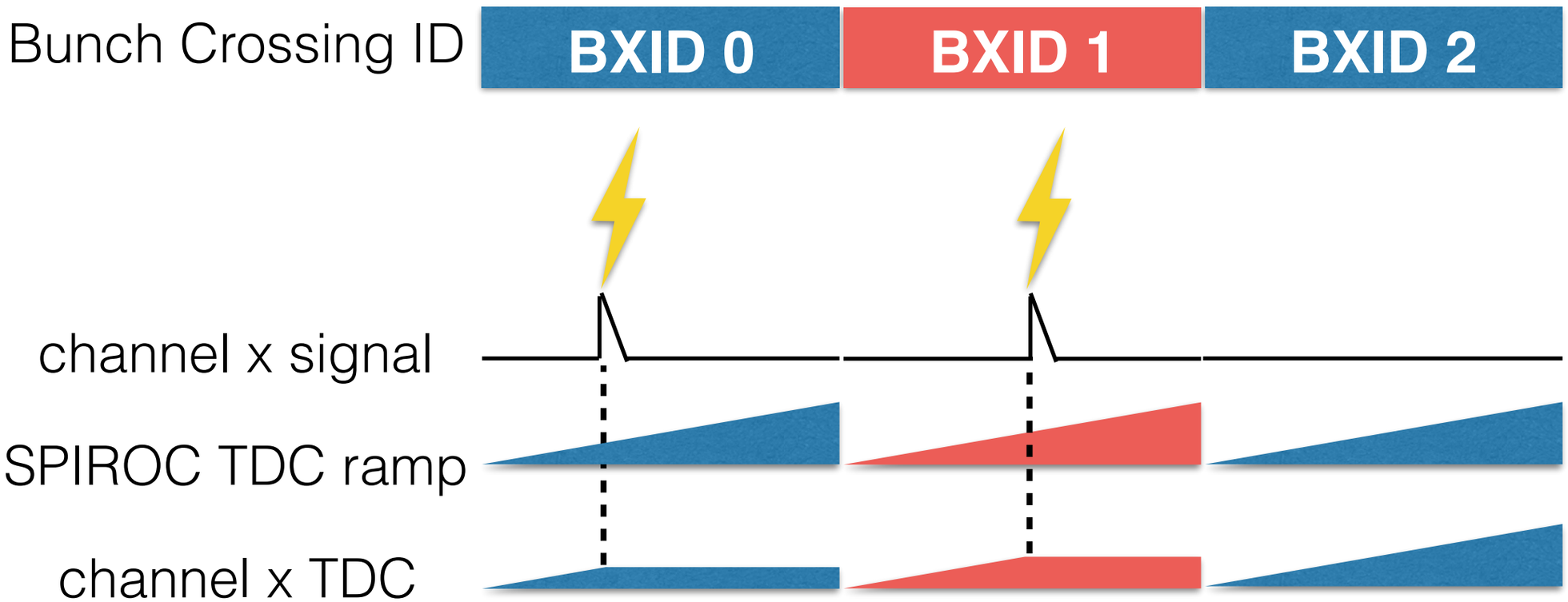
- Create a collection efficiency distribution that realize the measurement.
- The same simulation was performed for some variable bundle patterns.
- It was found that acceptable resolution (σ~4mm) was obtained with bundling every 16 fibers.

DAQ Diagram



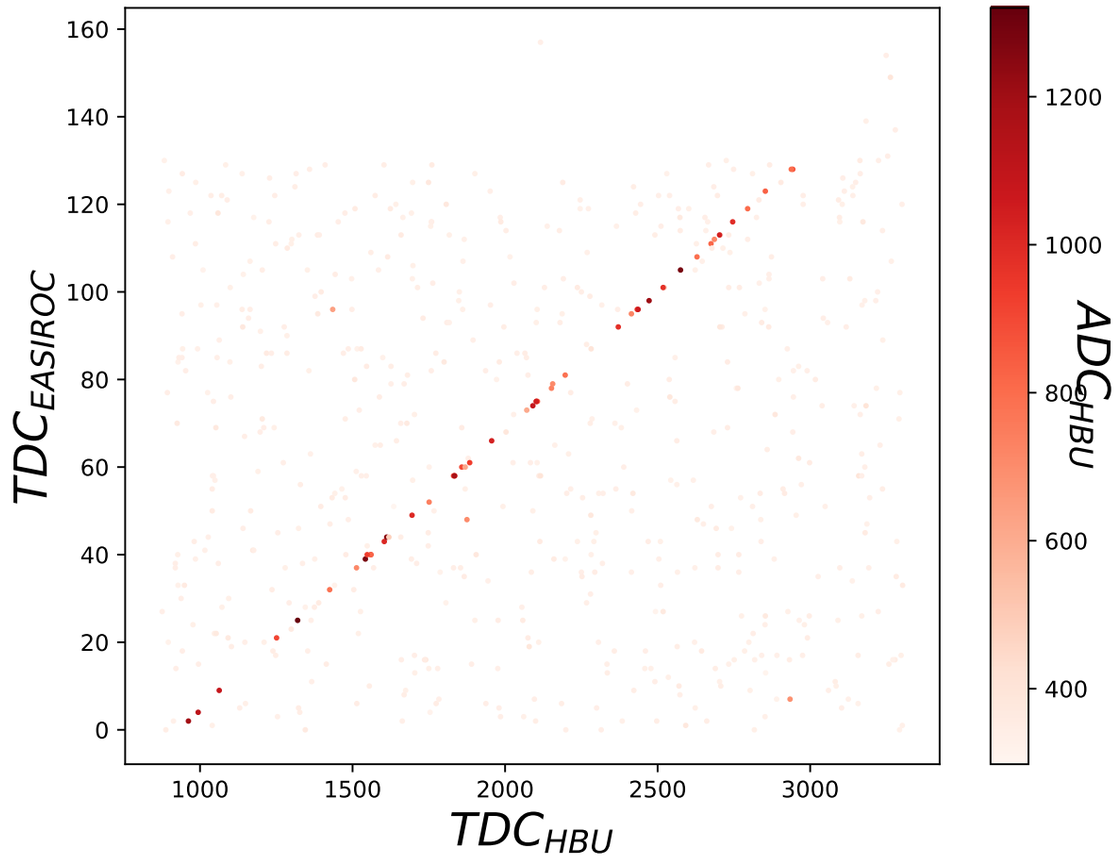
- Two kinds of module use the same clock that is provided by CCC
- and ACQ signal->EASIROC modules

HBU TDC



- There are two global TDC ramps in a SPIROC chip on a HBU.
- One is used at even bunch crossing
- Time information is stored in the analog memory cells by sampling and holding the global TDC ramp value.

Correlation with One Ramp



- Each ASIC chip uses two TDC ramps.
- We can see only one line in this figure: This corresponds to TDC with one ramp.

Interface Integration-EUDAQ

- EUDAQ is a data acquisition framework, written in C++
- We can take data from two modules by single interface - EUDAQ.
- By implementing an EASIROC producer, we will operate EASIROC modules almost in the same way as HBU, not separately.
- So far, we made the EASIROC producer and succeeded to operate two modules simultaneously by EUDAQ.
  - The development on the data collecting system is ongoing.